# Xyce™ Parallel Electronic Simulator
# Version 6.5 Release Notes

Sandia National Laboratories

June 2, 2016

The ***Xyce***™ Parallel Electronic Simulator has been written to support the simulation needs of Sandia National Laboratories' electrical designers. ***Xyce***™ is a SPICE-compatible simulator with the ability to solve extremely large circuit problems on large-scale parallel computing platforms, but also includes support for most popular parallel and serial computers.

For up-to-date information not available at the time these notes were produced, please visit the ***Xyce***™ web page at `http://xyce.sandia.gov`.

# Contents



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# New Features and Enhancements

## New Devices and Device Model Improvements

- BSIM6 and VBIC 1.3 enhancements with observed performance gains as high as 25% on some circuits.
- Xyce/ADMS Verilog-A model compiler code generation enhancements: improved support for (initial_model) and (initial_instance) blocks.
- Xyce/ADMS new feature: added support of white_noise and flicker_noise for use in small-signal noise analysis.
- Noise models have been added for all devices generated from Verilog-A using ADMS, except for the FBH HBT model.
- Support for tap-changing in the Power Grid Transformer model.
- The JUNCAP200 diode model has been added as Diode level 200.
- The MVS MOSFET model has been added as models level 2000 (ETSOI version) and 2001 (HEMT version).
- The BSIM3 and BSIM4 models can now output transconductance on the .PRINT line.

## Enhanced Solver Stability, Performance and Features

- Internal full-step Newton method is now the default for transient simulation, which improves memory efficiency and performance.
- Xyce has been updated to use Trilinos 12.6.3.
- Transient adjoint parameter sensitivities are now supported.
- NOTE: THE BDF TIME INTEGRATION METHOD (METHOD=BDF or METHOD=6) IS NOW DEPRECATED. It will be removed in version 6.6 of **Xyce**. The Trapezoid (METHOD=TRAP or METHOD=7) and Gear (METHOD=GEAR or METHOD=8) methods will be the only supported time integration methods in version 6.6. Please update any netlists you have that explicitly use the BDF time integration method to use the Gear method instead. If this results in convergence or accuracy issues, please contact the Xyce Development Team as soon as possible.

## Interface Improvements

- Improved support for RISE, FALL, CROSS and LAST qualifiers in .MEASURE statements.
- Re-measure now supports .CSD files and .STEP with .TRAN.
- Improved support for lead currents, expressions and power in .MEASURE and .FOUR statements.
- Restart can now provide seamless checkpointing for all time integration methods.
- Power calculations are now supported for the level 1 BJT.
- Improved output for restart result interpolations.

# Defects Fixed in this Release

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia users. SON, which is on the open network, and SRN, which is on the restricted network.

| Defect | Description |
|---|---|
| **791-SON** : SPICE_SIN expression function segfaults with only 3 arguments | A missing conditional would cause the SPICE_SIN function of the expression library to segfault if called with only the three mandatory arguments (offset, amplitude, frequency). The bug was fixed, and a test case is now in the test suite to prevent a regression. |
| **2007-SRN**: Xyce 6.4 (and some earlier versions) would overwrite the user's input netlist if both CSV output and continuation were requested | A flaw in the output system allowed the unique combination of CSV transient output and continuation solver options to overwrite the input netlist with homotopy output if no .print HOMOTOPY line were given. This is no longer possible, and a correctly functioning failsafe is in place at the lowest level of the output system to prevent it from ever attempting to write into the input netlist. |
| **777-SON**: Xyce binaries on OS X El Capitan cannot find shared libraries | A change in security features on OS X El Capitan rendered the use of the environment variable `DYLD_LIBRARY_PATH` ineffective. This caused older **Xyce** binaries to fail with missing shared library errors. The Xyce 6.5 binaries are built in a way so that this environment variable is no longer needed on OS X. |
| **526-SON and 527-SON**: The TO, FROM, DELAY and RISE/FALL/CROSS Features of .MEASURE Should Work For All Measures (where appropriate and even with noisy waveforms) | The support for these qualifiers is now documented in the Reference Guide and fully tested in the Regression Test suite. For noisy waveforms, the ability to explicitly set the "cross level" for the `AVG`, `DERIV`, `DUTY`,`FIND-WHEN`, `INTEG`, `MAX`, `MIN`, `PP`, `RMS` and `WHEN` measures was added via a new `RFC_LEVEL` qualifier. |
| **695-SON**: Support re-measure of .csd files | **Xyce** now supports re-measure of both `.prn` and `.csd` output files. However, re-measure might only work with .csd files generated by **Xyce**. |
| **696-SON**: Make re-measure work with .STEP | Both `.MEASURE` statements and re-measure now work with `.STEP` data generated by a transient (`.TRAN`) analysis. This now works for both `.prn` and `.csd` output files. |
| **698-SON**: Fix issues when I(), P() and W() are used in .MEASURE statements | `.MEASURE` statements would fail netlist parsing if the requested branch current was omitted from the `.PRINT TRAN` line. This is fixed now. |
| **703-SON**: Make P(), W(), N(), expressions and transistor lead currents work as the output variable (ov) on a .FOUR line | Support for P(), W(), N() and transistor lead currents on `.FOUR` lines was added for version 6.4 of **Xyce**. There were still two outstanding issues though. First, `.FOUR` statements would fail netlist parsing if the requested branch current was omitted from the `.PRINT TRAN` line. Second, expressions were not allowed on a .FOUR line. These last two issues are fixed now. |
| **719-SON**: Restart no longer does a seamless "as though the code never stopped" restart | Checkpointing and restarting in **Xyce** has been broken for many releases because not enough information was saved to restart a simulation "as though it had never stopped." Much work has been done to ensure that the restart file contains the necessary options and history for the time integration method used in the netlist that generates the restart file. So, now **Xyce** will truly restart the simulation "as though it had never stopped." |

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| Defect | Description |
|---|---|
| **721-SON**: Improve error handling for re-measure | In version 6.4 of **Xyce**, trying to re-measure either an invalid file or a valid file with an unsupported extension (e.g., re-measure anything other than .PRN format in version 6.4) would cause a core dump. This has been fixed now. |
| **722-SON**: Xyce-generated .CSD files for .TRAN data with .STEP do not open correctly in PSpice | The issue was that Xyce was not outputting a "complete header block" at the start of the data for each step. This is fixed now, and the Xyce-generated .CSD files open correctly in PSpice v16.6. |
| **724-SON**: Handle case of AT value in DERIV measure exactly equal to a time value in the output file | The `DERIV` measure would fail if the `AT` value was exactly equal to one of the time values in the output `.PRN` file. A simple example was:<br>`.OPTIONS OUTPUT INITIAL_INTERVAL=0.001`<br>`.MEASURE TRAN DERIV_AT DERIV V(1) AT=0.025`<br>This is fixed now, and the `AT` qualifier also works when it is equal to the beginning or ending simulation time. |
| **729-SON**: Add warning message for unsupported .DC and .AC measure statements | **Xyce** `.MEASURE` statements do not support `DC` or `AC` modes. In previous versions, measure statements like those given below would be run by **Xyce** but the results would typically not be correct. The new behavior is that **Xyce** still runs the netlist, but it now emits warning messages about the unsupported measure statements. **Xyce** does not produce any output for the unsupported AC or DC measures in either stdout or in the `.mt0` file.<br>`.MEASURE DC MAXDC MAX V(1)`<br>`.MEASURE AC MAXAC MAX V(1)` |
| **730-SON**: Xyce hangs when passed a directory instead of a netlist | **Xyce** did not detect when it was passed a directory path instead of a netlist file. So, when passed a directory path, **Xyce** got to the "Reading and parsing netlist..." phase, and hung. This has been fixed. |
| **769-SON**: Subcircuit interface nodes not printable in parallel for processors $> 3$ | Actually the problem is when a subcircuit interface node is referenced on the .PRINT line AND there are more MPI processors allocated than the number of devices in the circuit. This is because the alias list for this subcircuit node was not broadcast to all MPI processors. This has been fixed. |
| **775-SON**: Nonlinear mutual inductor fixed scaling parameters are ignored | The nonlinear mutual inductor model parameters for scaling the internal $M$ and $R$ variables were ignored if the user specified them. This has been fixed so that **Xyce** now uses any provided scaling via `MVARSCALING` and `RVARSCALING`. |
| **781-SON**: Restart output does not work with interpolations | When .options restart and .options output initial_interval are used together, the output between time 0 and restart time is wrong. This is fixed. |

# Interface Changes in this Release

Table 2: Changes to netlist specification since the last release.

| Change | Detail |
|---|---|
| The default value for the NL parameter for the lossless transmission line (T device) was changed | The default value for the NL (length in wavelengths) parameter for the lossless transmission line (T device) was changed from 0 to 0.25 wavelengths. This default value matches SPICE3f5 and PSpice. |
| `PRINT` qualifier added for `.MEASURE` lines. | This qualifier is available for all measure types It allows the user to control where the measure output appears (suppressed, stdout only, `.mt0` file only or both places). The default is both stdout and the `.mt0` file. |
| `OUTPUT` qualifier added for `.MEASURE` lines | This qualifier is only available for the `MAX` and MIN measure types. It allows the user to control whether the measure's value or time (i.e., the maximum value of the measured waveform or the time when that maximum value occurred) appears in the `.mt0` file. This qualifier does not affect the descriptive output for the measure that is printed to standard output. |

# Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|---|
| **783-SON**: Use of ddt in a B-Source definition may produce incorrect results | The `DDT()` function from the **Xyce** expression package, which implements a time derivative, may not function correctly in a B-Source definition.<br>***Workaround***: None. |
| **754-SON**: Problems with use of global parameters for DC source values | The internal handling of global parameters in expressions can interfere with the handling of DC source sweeps and "source stepping". It was not possible to fix this bug in time for Release 6.5, as the impact of changing the behavior is too broad.<br>***Workaround***: Do not use global parameters in expressions for the DC value of a voltage or current sources that are swept using a `.DC` analysis. Since any circuit which has to fall back on "source stepping" for DCOP convergence will not work as intended if any source has a global parameter for its DC value, it is advisable not to use global parameters at all in DC sources, even for sources that are not swept by a `.DC` analysis. |
| **718-SON**: Missing error message for invalid nodes in expressions on .PRINT lines | If an invalid node is specified on a **Xyce** `.PRINT TRAN` line then **Xyce** should return a fatal error during netlist parsing (e.g., `.PRINT TRAN V(BOGONODE)` will produce an error message of `undefined symbol in .PRINT command:  node BOGONODE`, if `BOGONODE` does not exist in the netlist). However, if the invalid node is inside a **Xyce** expression (e.g., `.PRINT TRAN {V(BOGONODE)}`) then **Xyce** will not produce an error message during netlist parsing and the output value for `{V(BOGONODE)}` will be zero for all time-steps.<br>***Workaround***: There is none, other than noticing that a output waveform value is unexpectedly all zeroes, and correcting the `.PRINT` statement. |
| **707-SON**: Behavior for invalid nodes on .FOUR lines and in .MEASURE statements | There are issues with `.FOUR` lines and `.MEASURE` statements that accidentally use node names that are not in the netlist. In that case, the `.cir.four` output file will contain a mix of all zero's and NaN's, and **Xyce** will not produce a warning or error message about the invalid node name. Similarly, the measure statement will run without a warning message about the invalid node name. The measure result will then be zero, rather than FAILED. |
| **704-SON**: Lead currents do not work in AC analyses, crash **Xyce** | Lead currents for devices other than voltage sources are not solution variables, and are computed by **Xyce** as a derived quantity in a post-processing step. This is not set up correctly to work when doing small-signal AC analysis. Attempting to print such a lead current or any of its computed quantities (magnitude, phase, real or imaginary parts) will cause **Xyce** to crash. The lead currents do work as expected in time-domain analysis such as transient and DC. Lead currents work properly in HB frequency-domain analysis.<br>***Workaround***: Do not attempt to print currents through a device other than a voltage source in any AC simulation. If you need the current through a device under AC analysis, place a zero-volt voltage source in series with that device, and print the current through the voltage source. |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|---|
| **667-SON** Make `.IC` and `.NODESET` usable inside subcircuits | `.IC` and `.NODESET` statements within subcircuits are silently ignored by **Xyce**. ***Workaround***: The `.IC .NODESET` sections of the **Xyce** Reference Guide describe how to work around this bug by moving the statements to the top-level of the circuit. |
| **661-SON** Branch Currents and Power Accessors (I(), P() and W()) Do Not Work Properly in .RESULT Statements | There are two issues. First, `.RESULT` statements will fail netlist parsing if the requested branch current is omitted from the `.PRINT TRAN` line. As an example, this statement (`.RESULT I(R1)`) requires either `I(R1)`, `P(R1)` or `W(R1)` to be on the `.PRINT TRAN` line. Second, the output value, in the `.res` file, for the lead current or power calculation will always be zero. |
| **652-SON**: HB output is buggy | While a straightforward use of `.print HB` works as described in the users and reference guides, several of the documented features do not work as intended.<br>`.print HB_FD` and `.print HB_TD` are intended as a way of specifying variable lists for frequency- and time-domain outputs, respectively. It has been discovered that these only produce output if there are print specifications for *both* frequency and time domain. That is, if only one of `.print HB_FD` or `.print HB_TD` is present in the netlist, no output will be produced at all. This bug was discovered too late to be fixed in time for release 6.4.<br>***Workaround***: When performing harmonic balance analysis, always specify enough print lines so that both time- and frequency-domain variables are output. This could be by specifing `.print HB` alone, by specifying both `.print HB` and `.print HB_TD`, or by specifying both `.print HB_FD` and `.print HB_TD`. |
| **583-SON**: Switch with RON=0 leads to convergence failure. | The switch device does not prevent a user from specifying `RON=0` in its model, but then takes the inverse of this value to get the "on" conductance. The resulting invalid division will either lead to a division by zero error on platforms that throw such errors, or produce a conductance with "Not A Number" or "Infinity" as value. This will lead to a convergence failure.<br>***Workaround***: Do not specify an identically zero resistance for the switch's "on" value. A small value of resistance such as 1e-15 or smaller will generally work well as a substitute. |
| **469-SON**: Belos memory consumption on FreeBSD and excessive CPU on other platforms | Memory or thread bloat can result when using multithreaded dense linear algebra libraries, which are employed by Belos. If this situation is observed, either build **Xyce** with a serial dense linear algebra library or use environment variables to control the number of spawned threads in a multithreaded library. |
| **468-SON**: It should be legal to have two model cards with the same model name, but different model types. | SPICE3F5 and ngspice only require that model cards of the same type have unique model names. They accept model cards of different types with the same name. **Xyce** requires that all model card names be unique. |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|---|
| **250-SON**: NODESET in **Xyce** is not equivalent to NODESET in SPICE | As currently implemented, `.NODESET` applies the initial conditions given throughout a full nonlinear solve for the operating point, then uses the result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to **Xyce**'s `.NODESET` failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround. |
| **247-SON**: Expressions don't work on .options lines | Expressions enclosed in braces ({ }) are handled specially throughout **Xyce**, and may only be used in certain contexts such as in device model or instance parameters or on `.PRINT` lines. |
| **49-SON Xyce** BSIM models recognize the model TNOM, but not the instance TNOM | |
| **37-SON**: Connectivity checking is broken for devices with more than 10 leads | The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If your circuit has that type of large, highly-connected mutual inductor and the code exits with an error message, this bug may be the source of the problem. The error message now includes a recommendation to use the workaround below.<br>***Workaround***: Disable connectivity checking by adding the line<br>`.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0`<br>to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor. |
| **27-SON**: Fix handling of .options parameters | When specifying .options for a particular package, what gets applied as the non-specified default options might change. |
| **1962-SRN**: Voltages from interface nodes for subcircuits may not work correctly in expressions on `.PRINT` lines | An expression that uses a voltage from an interface node to a subcircuit on a `.PRINT` line may only work if that voltage node is also used outside of the expression on the `.PRINT` line. A simple example is as follows. The expression `{V(X1:a)*I(X1:R1)}` prints out as 0, unless `V(X1:a)` is also on the `.PRINT` line. |
| **1923-SRN**: LC lines run out of memory, even if equivalent (larger) RLC lines do not. | In some cases, circuits that run fine using an RLC approximation for a transmission line, exit with an out-of-memory error if the (supposedly smaller) LC approximation is used. |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|---|
| **1903-SRN**: **Xyce** fails to collect several inductors into a linear mutual inductor | In some rare cases with complex include file usage, the mutual inductor syntax with multiple couplings can fail to work. **Xyce** will return an error message that it can not find `L_L1`:<br>`L_L1 node1 node1 inductance1`<br>`L_L2 node3 node4 inductance2`<br>`L_L3 node5 node6 inductance3`<br>`L_L4 node7 node8 inductance4`<br>`K_K1 L_L1 L_L2 L_L3 L_L4 .999` |
| **1595-SRN**: **Xyce** won't allow access to inductors within subcircuits for mutual inductors external to subcircuits | It is not possible to have a mutual inductor outside of a subcircuit couple to inductors in a subcircuit.<br>***Workaround***: Put all inductors and mutual inductance lines that couple to them together at the same level of circuit hierarchy. |

# Supported Platforms

## Certified Support

The following platforms have been subject to certification testing for the **Xyce** version 6.5 release.

- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X Yosemite, x86-64 (serial and parallel)

Note that the **Xyce** team has dropped Certified Support for Red Hat Enterprise Linux® 5. RHEL5 is now in the "Build Support" category.

## Build Support

Though not certified platforms, **Xyce** has been known to run on the following systems.

- FreeBSD 9.x and 10.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux 6
- Microsoft Windows under Cygwin and MinGW.

# **Xyce** Release 6.5 Documentation

The following **Xyce** documentation is available on the **Xyce** website in pdf form.

- **Xyce** Version 6.5 Release Notes (this document)
- **Xyce** Users' Guide, Version 6.5
- **Xyce** Reference Guide, Version 6.5
- **Xyce** Mathematical Formulation
- Application Node: Using Open Source Schematic Capture Tools with **Xyce**

Also included at the **Xyce** website as web pages are the following.

- Building Guide (instructions for building Xyce from the source code)
- Running the Xyce Regression Test Suite
- Frequently Asked Questions

# External User Resources

- Website: http://xyce.sandia.gov
- Google Groups discussion forum: https://groups.google.com/forum/#!forum/xyce-users
- Email support: xyce@sandia.gov
- Address:

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