Xyce™ Parallel Electronic Simulator
Version 7.6 Release Notes

Sandia National Laboratories

October 24, 2022

The **Xyce**™ Parallel Electronic Simulator has been written to support the simulation needs of Sandia National Laboratories' electrical designers. **Xyce**™ is a SPICE-compatible simulator with the ability to solve extremely large circuit problems on large-scale parallel computing platforms, but also includes support for most popular parallel and serial computers.

For up-to-date information not available at the time these notes were produced, please visit the **Xyce**™ web page at `http://xyce.sandia.gov`.

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Xyce™
PARALLEL ELECTRONIC SIMULATOR

New Features and Enhancements

XDM

- XDM now allows models to be redefined within the same scope without raising an exception. Previously, the code would exit out if a model was redefined. Now, it will just emit a warning.

- XDM now tranlates the SPECTRE model parameter "VERSION" to "version".

- HSPICE expressions can be delimited by double quotes. XDM would either let this pass through without making any changes (which would cause problems with the resultant Xyce netlist), or comment it out in some cases (mostly, in expressions in sources). This was fixed by adding a HSPICE grammar rule that defines expressions delimited by double quotes, and then adding code in the parser interface to change the expression delimiters to curly braces.

New Devices and Device Model Improvements

- The voltage-controlled current source (VCCS, or 'G' device) now supports the M multiplier parameter.

- The BSIM4 device (level 14 and 54 MOSFET) now supports three versions, the 4.6.1 version that has been present for many releases and the 4.7.0 and 4.8.2 versions new to this release. The specific version of BSIM4 can be selected by setting the VERSION parameter on the .MODEL line for the device. At this time the BSIM4 is the only device in Xyce that supports multiple versions in this manner.

Enhanced Solver Stability, Performance and Features

- The new harmonics selection method based on diamond truncation has been added for HB analysis.

- Improvements to the parser have been made to address significant slowdowns in processing the open source SkyWater 130nm PDK. For exemplar stress tests, parsing is now up to 20x faster.

Interface Improvements

- The number of warnings output by Xyce can now be controlled by the command-line option "-max-warnings #". The default maximum number of warnings is now 100, before it was unlimited.

Important Announcements

- The model interpolation technique described in the Xyce Reference Guide in section 2.1.18 has been marked as deprecated, and will be removed in a future release of Xyce.

Defects Fixed in this Release

Table 1: Fixed Defects. The Xyce team has multiple issue trackers, and the table below indicates fixed issues by indentifying both the tracker and the issue number. Further, some issues are reported by open source users on GitHub and these issues may be tracked using multiple issue numbers.

Defect	Description
Xyce Backlog Bugs/1: Mutual inductor jacobian error	A jacobian term in the nonlinear mutual inductor was wrong when the bias was changing across the primary inductor. This jacobian error could lead to slower nonlinear convergence in transient simulations. It has been fixed.
Xyce Backlog Bugs/2: Mutual inductors have a bad device connectivity map	The device connectivity map is used to determine the path to ground for error checking. The linear and nonlinear mutual inductors were not correctly setting up the device connectivity map and this resulted in false warnings that some circuit nodes did not have a path to ground. The warning was invalid and this issue did not effect Xyce's calculations. But the warning was incorrect and could cause confusion. The code has been fixed and this warning should no longer appear under false conditions.
Xyce Backlog Bugs/7: Infinite loop results when ".ends" is missing from netlist	If a netlist ended without closing a subcircuit with ".ends" and ".end" was not used to signify the end of the netlist, then Xyce would either execute an infinite loop or seg fault. The parser now identifies this error and cleanly exits the simulation with an informative message.
Xyce Backlog Bugs/8: MOSFET multiplicity not applied to noise	None of the legacy MOSFETs (level 1,2,3, 6, 9(BSIM3) and 14 (BSIM4)) in Xyce were correctly applying the multiplicity factor ("M=") to noise terms. They do now.
Xyce Backlog Bugs/19: Error in the failure history output by Xyce in parallel	A runtime error was observed in the failure history output when the node name string was not available on the processor accessing the string. The character string is now being broadcast from the processor that owns the character string to all other processors.
Xyce Project Backlog/474: Remove spice-incompatible breakdown parameter algorithm from level 1 and 2 diode	When a user specifies both IBV and BV to the diode, an iterative technique is employed to assure that the forward and reverse regions match, which can adjust the breakdown voltage if necessary. The SPICE3F5 algorithm may or may not converge, and can sometimes produce unreasonable solutions to the matching problem. In 2007 an improved algorithm was devised and implemented in the Xyce diode, but this broke strict SPICE compatibility. This algorithm has been reverted to the SPICE-compatible method. Some small differences in simulation results as compared to prior versions of Xyce may result from this change, but the changes will make the results more compatible with those from other simulators.

Table 1: Fixed Defects. Note that we have two multiple issue tracking systems for Sandia Users. SON and SRN refer to our legacy open- and restricted-network Bugzilla system, and Gitlab refers to issues in our gitlab repositories.

Defect	Description
Xyce Project Backlog/471: Removal of spice-incompatible IRF parameter from diode	The Xyce diode has, since 2005, supported a Xyce-specific, SPICE3F5 incompatible parameter called `IRF` that purported to allow a user to fudge the reverse current expression to match experimental data. Though the original implementation was intended to fall back to strict SPICE3F5 compliance when `IRF` was not specified, later development broke it and led to non-physical, temperature-dependent discontinuities in the diode formulation even when `IRF` was not specified. In Xyce 6.11 we fixed the fall-back behavior, but marked the parameter as deprecated and had Xyce report a warning if it was specified. As of Xyce 7.6 this feature has been completely removed, restoring strict SPICE3F5 compatibility.
Xyce Project Backlog/260: Fix version string in CMake development builds	Xyce reports its version using `Xyce -v`. With development versions of Xyce, the reported version should include the Git SHA against which the code was compiled along with the time of compilation. Prior to this change, CMake would include the SHA and time at *configure* time, not compilation time. That is now fixed.
Xyce Project Backlog/285: CMake support for XyceCInterface	The C-interface to the C++ object N_CIR_Xyce did not have the needed files for building under CMake. This issue has been resolved and the C-interface is now built and installed as part of Xyce.
Xyce Project Backlog/302: Xyce legacy MOSFETs do not recognize VT0	Xyce did not properly recognize that VT0 should be an alias for VTO in the levels 1 through 6 legacy MOSFET devices. These have been recognized by every SPICE derivative since SPICE3 (though were not recognized by SPICE2), and are now recognized by Xyce, too.
Xyce Project Backlog/151: Xyce reports error "Directory node not found"	Xyce reports this error when non-existent solution nodes being referred to by circuit devices and cannot be resolved. The simulator now provides a more informative error that indicates which solution node has not been resolved and what device refers to this node.
Xyce Project Backlog/419, 420, 352: Xyce only supports version 4.6.1 of the BSIM4	Until now, Xyce only supported version 4.6.1 of the BSIM4 and ignored any setting of the `VERSION` parameter in the model card for level 14 or 54. As of this release, Xyce supports multiple versions (4.6.1, 4.7.0, and 4.8.2), all specified as level 14 or 54 and selected by the `VERSION` parameter in the model card. The BSIM4 is currently the only device in Xyce that supports multiple versions in this manner.
Xyce Project Backlog/448: Auger recombination function used by the TCAD (PDE) devices is scaled incorrectly	The Auger recombination term used by the TCAD devices in Xyce was scaled incorrectly, and this resulted in that term being nearly zero. This has been corrected.
Xyce Project Backlog/455: Xyce gives a bad error message for malformed voltage source	Under some circumstances, a grammar mistake in the netlist specification of an independent source caused Xyce to exit with a fatal error, but with an incomprehensible error message. This has been corrected.

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Defect	Description
Xyce Project Backlog/bugs/23: Fix the Philips mobility model for the TCAD devices	The Philips mobility model had a bug in it that resulted in NaNs being produced during an intermediate calculation. The model would discard these NaNs under most circumstances. However, they were computed inside of a while loop, and on some compilers these NaNs prevented the while loop from exiting. This model has been completely rewritten and this behavior will no longer occur.
Xyce Project Backlog/264: Modify Xyce CMake to use the modern CMake in Trilinos	Trilinos 13.5 introduces support for modern CMake targets. As part of the transition to CMake targets, several Trilinos defined CMake variables have been marked as deprecated (including some variables containing library names, library paths, and include directories). When building Xyce from source with CMake, dependencies in Trilinos are now referenced through Trilinos provided CMake targets (instead of explicitly using library names and paths). These CMake build system changes are not backwards compatible; the CMake scripts require Trilinos 13.5 or greater to build Xyce.

Supported Platforms

Certified Support

The following platforms have been subject to certification testing for the Xyce version 7.6 release.

- Red Hat Enterprise Linux$^{®}$ 7, x86-64 (serial and parallel)

- Microsoft Windows 10$^{®}$, x86-64 (serial)

- Apple$^{®}$ macOS, x86-64 (serial and parallel)

Build Support

Though not certified platforms, Xyce has been known to run on the following systems.

- FreeBSD 12.X on Intel x86-64 and AMD64 architectures (serial and parallel)

- Distributions of Linux other than Red Hat Enterprise Linux 6

- Microsoft Windows under Cygwin and MinGW

Xyce Release 7.6 Documentation

The following Xyce documentation is available on the Xyce website in pdf form.

- Xyce Version 7.6 Release Notes (this document)

- Xyce Users' Guide, Version 7.6

- Xyce Reference Guide, Version 7.6

- Xyce Mathematical Formulation

- Power Grid Modeling with Xyce

- Application Note: Coupled Simulation with the Xyce General External Interface

- Application Note: Mixed Signal Simulation with Xyce 7.2

Also included at the Xyce website as web pages are the following.

- Frequently Asked Questions

- Building Guide (instructions for building Xyce from the source code)

- Running the Xyce Regression Test Suite

- Xyce/ADMS Users' Guide

- Tutorial: Adding a new compact model to Xyce

External User Resources

- Website: http://xyce.sandia.gov

- Google Groups discussion forum: https://groups.google.com/forum/#!forum/xyce-users

- Email support: xyce@sandia.gov

- Address:

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