

Xyce™ Parallel Electronic Simulator Version 6.8 Release Notes

Sandia National Laboratories

October 18, 2017

The Xyce™ Parallel Electronic Simulator has been written to support the simulation needs of Sandia National Laboratories' electrical designers. Xyce™ is a SPICE-compatible simulator with the ability to solve extremely large circuit problems on large-scale parallel computing platforms, but also includes support for most popular parallel and serial computers.

For up-to-date information not available at the time these notes were produced, please visit the Xyce™ web page at <http://xyce.sandia.gov>.

Contents

| | |
|--|-----------|
| New Features and Enhancements | 2 |
| Defects Fixed in this Release | 3 |
| Interface Changes in this Release | 6 |
| Known Defects and Workarounds | 7 |
| Supported Platforms | 11 |
| Xyce Release 6.8 Documentation | 11 |
| External User Resources | 12 |



New Features and Enhancements

New Devices and Device Model Improvements

- A code optimization of the BSIM-CMG model 110 (MOSFET level 110) has improved performance of this model when self-heating effects are disabled by setting SHMOD=0 or RTH=0 in the .model card.
- The VBIC 1.2 (Level=10) model has been deprecated since **Xyce** Release 6.6. It is still available in **Xyce** 6.8, but is unmaintained and will be removed in a future release. To remind users that this model is slated for future removal, **Xyce** will show the text “**DEPRECATED**” next to the model name in its device count summary.

The VBIC 1.3 model (levels 11 and 12) will be the only supported VBIC models in the future. Please update any netlists you have that use the level=10 model to use one of these VBIC 1.3 models instead. See the **Xyce** Reference Guide for details on the differences between the 1.2 and 1.3 versions of VBIC.

Users are advised to update their VBIC netlists as soon as possible.
- The Piecewise Empirical Model (PEM) memristor model has been added to **Xyce**. See the **Xyce** Reference Guide for details.

Enhanced Solver Stability, Performance and Features

- The BDF time integration method (METHOD=BDF or METHOD=6) has been deprecated since version 6.6 of **Xyce**, and has been removed in this release. The Trapezoid (METHOD=TRAP or METHOD=7) and Gear (METHOD=GEAR or METHOD=8) methods are the only supported time integration methods in version 6.8. Please update any netlists you have that explicitly use the BDF time integration method to use the Gear method instead.
- Improved robustness of GMIN stepping and SPICE DC OP strategy.

Interface Improvements

- The CSV print format is now supported for homotopy and noise output.
- A new GNUPLOT print format that outputs data in standard columns, like a .prn file, but with improved Gnuplot compatibility for .STEP data.

Deployment Improvements

- The wrapper scripts `runxyce` and `xmpirun` are no longer provided by our packaged installers. **Xyce** is now run directly without the use of these scripts. For details please see the **Xyce** Users' Guide.
- This version of **Xyce** has been built against the latest released version 12.12.1 of Trilinos.
- **Xyce** no longer requires the UMFPACK library for serial builds and neither UMFPACK nor ParMETIS are required for parallel builds.

Defects Fixed in this Release

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia users. SON, which is on the open network, and SRN, which is on the restricted network.

| Defect | Description |
|--|---|
| 896-SON: Do away with “runxyce” and “xmpirun” scripts entirely | The <code>runxyce</code> and <code>xmpirun</code> scripts were historical artifacts dating back to early versions of Xyce . They were present only in released binary installs of the code, which required us to document two different methods of running the code depending on whether a user had installed via source or via binary installers. Furthermore in recent releases have been doing nothing but invoking the Xyce binary directly, and the scripts have actually been unnecessary since Xyce Release 6.6. These scripts have been removed entirely, and now users of Xyce invoke the code in the same way whether they are installing from source or from binary distributions. |
| 28-SON: Problems with parameter resolution when mutual inductors exist in subcircuits | When a subcircuit contained mutual inductors, a bug in the input parser's context resolution code led Xyce to report incorrect errors regarding unrecognized symbols. The error in context resolution has been fixed, and these error messages are no longer generated. |
| 913-SON: “Unmatched parentheses” error when certain words are used as parameter names | The implementation of “vector composite parameters” as used by a small number of special devices led to 15 specific parameter names being unavailable for use as user defined parameters in <code>.PARAM</code> statements if the parameter value was an expression enclosed in curly braces. These parameters were <code>DOPINGPROFILES</code> , <code>SOURCELIST</code> , <code>LAYER</code> , <code>REGION</code> , <code>NODE</code> , <code>RXNREGION</code> , <code>COIL</code> , <code>FIELDATA</code> , <code>PARAM</code> , <code>MM_CURRENT</code> , <code>MM_INDVARS</code> , <code>MM_INDFEQUS</code> , <code>MM_INDQEQUS</code> , <code>MM_FUNCTIONS</code> , and <code>MM_PARAMETERS</code> . Due to a bug in handling of these special names, if one used these names as the name of a parameter in a <code>.PARAM</code> statement with a value that is an expression enclosed in curly braces (“{”}) then Xyce would emit an unhelpful “Unmatched parentheses” error. The parser handling of vector composite was improved and these parameter names no longer behave as if they were reserved words. |
| 646-SON: <code>.csd</code> format for <code>PROBE</code> output is incorrect for specific numbers of output variables for <code>.AC</code> analyses | This line (<code>.PRINT AC FORMAT=PROBE V(1) V(2) V(3) V(4)</code>) would produce an incorrectly formatted <code>.csd</code> file that would not open in PSpice 16.6. In general, the bug occurred for <code>.AC</code> analyses if the number of output variables (N) on the <code>.PRINT AC FORMAT=PROBE</code> line satisfied this equation: $(N+1) \bmod 5 = 0$. This bug was fixed for <code>.TRAN</code> and <code>.DC</code> analyses for version 6.4 of Xyce . It is now also fixed for <code>.AC</code> analyses. |

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

| Defect | Description |
|---|---|
| <p>785-SON: Xyce hangs in parallel when passed a directory rather than a file</p> | <p>This bug was related to SON Bug 730 (“Xyce hangs when passed a directory instead of a netlist”), which was fixed in Xyce 6.5. Further testing showed that Xyce would hang (during parallel execution) if a directory name was used, rather than a file name, in .LIB or .INC statements. Xyce might also hang in parallel, or silently not produce the requested file in both serial and parallel, if the “output file” was either a directory or a file in a non-existent directory. (Note: the Xyce outputters will not create new subdirectories.) That could happen with either the FILE= keyword on a .PRINT line or with the -o, -l or -rsf command line options. These issues are fixed now. In addition, the error messages for all invalid input/output file names should be clearer now.</p> |
| <p>843-SON: Use of .STEP with .NOISE does not result in a complete output (.NOISE.prn) file</p> | <p>When .STEP was used with .NOISE, the output file would not contain the simulation results for all of the requested steps. This is fixed now.</p> |
| <p>850-SON: Segfault and improper error handling for improperly formatted functions</p> | <p>When a user-defined function was called with the wrong number of parameters, Xyce was supposed to abort with an error message. However, in some cases Xyce segfaulted instead. There were also cases where Xyce would improperly run a simulation with an incomplete argument list for a user-defined function. This is fixed now.</p> |
| <p>903-SON: .csd format for probe output is incorrect for large numbers of output variables (e.g., for V(*))</p> | <p>This bug was found via a .PRINT TRAN FORMAT=PROBE V(*) line that effectively output over 1000 variables. The resultant Xyce-generated .csd file would not open correctly in the PSpice A/D waveform viewer. The issue appeared to be a limit on the number of characters that could be on a single line in the #N (variable names) section of the .csd file header. Xyce now limits the length of those lines. So, this bug is fixed now, with the caveat that an extremely long variable name (e.g., > 400 characters) might still cause problems.</p> |
| <p>909-SON: Fix core dump for PWL source with FILE specified</p> | <p>This instance line (VPWL1 1 0 PWL FILE), where the file name for the Piecewise Linear (PWL) source specification is missing, would cause a core dump. This is fixed now.</p> |
| <p>912-SON: Fix core dump for .PRINT HOMOTOPY FORMAT=PROBE</p> | <p>Xyce would core dump if a homotopy occurred and the print format was FORMAT=PROBE. That could occur during a transient simulation, using .PRINT TRAN FORMAT=PROBE, even if there was no .PRINT HOMOTOPY line in the netlist. This is fixed now. The Xyce-generated .HOMOTOPY.csd files are now viewable within PSpice A/D with the caveats given in the Known Defects Table for SON Bug 939.</p> |
| <p>631-SON: In support of memristor modeling needs, the TEAM, Yakopcic and PEM memristor models have been added to Xyce</p> | <p>See the reference guide for details on the individual models.</p> |
| <p>933-SON: Xyce fails to run with Belos as the linear solver if singleton filtering reduces linear system to have zero rows</p> | <p>This bug is related to SON Bug 141 (which was fixed in Xyce 6.0), where this issue was resolved and tested for the AztecOO linear solver. The issue is that Xyce uses transformations to redistribute and permute the linear system. For some circuits, these transformations result in a trivial linear system or generate a permutation that causes problems for the iterative solvers. This is fixed now.</p> |

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

| Defect | Description |
|---|---|
| 805-SON: Parser fails to collect linear mutual inductors in an include file | Xyce would fail to collect component inductors together, into a mutual inductor, when they were in an include file rather than in the top-level netlist file. This is fixed now. |
| 1903-SRN: Xyce fails to collect several inductors into a linear mutual inductor | Xyce was failing to collect linear mutual inductors defined in included files. This was an issue with netlist parsing and has been resolved. |
| 907-SON: Xyce parser fails to handle hierarchical .lib statements | Xyce was failing to parse .lib statements that are found within other .lib files. This has been fixed and the parser can handle more complex hierarchical .lib parsing now. |
| 2073-SRN: Xyce could segfault, when .PRINT lines had no variables specified on them | <p>Xyce could segfault when there were multiple .PRINT lines for the same analysis type in a netlist, and one of them had no variables on it. A simple example was:</p> <pre data-bbox="748 699 1008 751">.PRINT TRAN V(1) V(2) .PRINT TRAN</pre> <p>This is fixed now.</p> |
| 946-SON: GMIN stepping does not work with .IC in some cases | The GMIN stepping homotopy method did not work with .IC if it was specified using continuation=1. The .IC is ignored. This is fixed now. |
| 947-SON: SPICE strategy does not initialize properly | The SPICE strategy uses Newton first, and then GMIN stepping and source stepping continuation methods. It did not initialize properly for each method and so could fail with the automatic SPICE strategy, but converge with the same source stepping when specified explicitly. This is fixed now. |

Interface Changes in this Release

Table 2: Changes to netlist specification since the last release.

| Change | Detail |
|--|---|
| The <code>FORMAT=RAW</code> print format for homotopy output has changed | The <code>FORMAT=RAW</code> print format is still unsupported for homotopy output. However, it now defaults to <code>FORMAT=STD</code> with the file extension of <code>.HOMOTOPY.prn</code> . In earlier versions of Xyce , the file extension was <code>.HOMOTOPY.unknown</code> . |
| The <code>FORMAT=PROBE</code> and <code>FORMAT=RAW</code> print formats for noise output have changed | Those two print formats are still unsupported for noise output. However, they now default to <code>FORMAT=STD</code> with the file extensions of <code>.NOISE.prn</code> . In earlier versions of Xyce , their file extensions were <code>.NOISE.unknown</code> . |
| A <code>.PRINT HOMOTOPY</code> line is now required to get homotopy output during a <code>.transient</code> simulation | In previous versions of Xyce , the contents of the <code>.PRINT TRAN</code> line was used to generate homotopy output during a transient simulation if there was no <code>.PRINT HOMOTOPY</code> line in the netlist. An explicit <code>.PRINT HOMOTOPY</code> line is now required for all analyses types in order to generate Xyce homotopy output. |
| The simulation footers for <code>.PRINT HOMOTOPY</code> and <code>.PRINT SENS</code> have changed slightly | For the <code>FORMAT=STD</code> , <code>FORMAT=GNUPLLOT</code> and <code>FORMAT=TECPLOT</code> print formats, <code>.PRINT HOMOTOPY</code> will now print the simulation footer "End of Xyce(TM) Homotopy Simulation" for all simulations (with and without <code>.STEP</code>). Similarly, <code>.PRINT SENS</code> will now print the simulation footer "End of Xyce(TM) Sensitivity Simulation" for all simulations (with and without <code>.STEP</code>). |

Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|--|
| <p>939-SON: Invalid fields (XBEGIN, XEND and SUBTITLE) in Xyce-generated .HOMOTOPY.csd files</p> | <p>The fields in the #H header block of the .HOMOTOPY.csd files are currently hard-coded to 0 and 1, respectively. The SUBTITLE field is incorrect for .STEP data. It is missing the values for the stepped parameters. Workaround: There is no workaround for the XBEGIN and XEND issue. However, it should not affect the “viewability” of those files in the PSpice A/D viewer. The workaround for the SUBTITLE issue is to put the stepped parameters on the .PRINT HOMOTOPY line.</p> |
| <p>928-SON: The .hb.ic.prn file can be incorrect when .STEP is used with .HB</p> | <p>Xyce should only output the initial condition (ic) data for the accepted tolerance in the <netlist-name>.hb.ic.prn file. However, it currently outputs all of the intermediate ic data while harmonic balance tries to find a good tolerance if .STEP is used with .HB. Workaround: There is no workaround.</p> |
| <p>911-SON: Improve compatibility of multi-file output with the -o command line option</p> | <p>If Xyce is invoked with the -o command line option then the output may be “interleaved” in one file rather than appearing correctly in multiple files. For example, if the netlist example.cir has these two .PRINT lines:</p> <pre>.PRINT TRAN V(1) .PRINT HOMOTOPY V(1)</pre> <p>and is invoked with Xyce -o output.text example.cir then the output that would normally appear in separate example.cir.prn and example.cir.HOMOTOPY.prn files would be jumbled together in the single file output.txt. This may not be what the user intended. Workaround: There are two workarounds. First, don't use -o if your netlist could output more than one file. Instead, use separate FILE= qualifiers on every .PRINT line. Second, use -o if desired but add FILE= to every .PRINT line other than .PRINT TRAN and .PRINT DC lines in your netlist.</p> |
| <p>883-SON .PREPROCESS REPLACEGROUND does not work on nodes referenced in expressions</p> | <p>The .PREPROCESS REPLACEGROUND feature does not replace ground synonyms if they appear in B source expressions. Workaround: There is none.</p> |
| <p>855-SON: Missing error message when a netlist uses an operator (e.g., IR or P) that is not supported for .AC analyses</p> | <p>This is related to SON Bug 718. Xyce will output all zeroes or all NaNs, for the requested quantity, when a netlist uses an operator (e.g., IR or P) that is unsupported for .AC analyses. Instead, Xyce should report a netlist-parsing warning or error for this case. Workaround: There is none, other than noticing that an output waveform value is unexpectedly all zeroes or all NaNs.</p> |
| <p>812-SON: Undocumented limitations on, and bugs with, parameter and global parameter names</p> | <p>Based on external customer input and pre-release testing, there are some bugs and undocumented limitations on parameter and global parameter names in Xyce. Parameters and global parameters should start with a letter, rather than with a number or “special” character like #. In addition, the use of a single character V as a global parameter name can result in either netlist parsing failures or incorrect results from .PRINT lines.</p> |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|--|---|
| 807-SON: BSIM4 convergence problems with non-zero rgatemod value | There have been reports of convergence problems (e.g., the Xyce simulation fails part way through and says that the “time step is too small”) when the <code>rgatemod</code> parameter is non-zero. |
| 794-SON: Bug in TABLE Form of Xyce Controlled Sources | In some case, a Xyce netlist with a controlled source, that uses the TABLE form, will get the correct answer at first. However, it may then “stall” (e.g, keep taking really small time-steps) and never complete the simulation run. Workaround: In some cases, the TABLE specification for the controlled source can be replaced with a Piecewise Linear (PWL) source that uses nested IF statements. |
| 783-SON: Use of <code>ddt</code> in a B-Source definition may produce incorrect results | The <code>DDT()</code> function from the Xyce expression package, which implements a time derivative, may not function correctly in a B-Source definition. Workaround: None. |
| 727-SON: Xyce parallel builds hang randomly on OS X | During Sandia’s internal nightly testing of the OSX parallel builds, we see that Xyce “hangs on exit” with an estimated frequency of less than 1-in-5000 simulation runs. We have not seen this issue with parallel builds for either RHEL6 or BSD. The hang is on exit, whether on a successful exit or on an error exit. The hang occurs after all of the Xyce output has occurred though. So, the user will get their sim results, but might have trouble if the individual Xyce runs are part of a larger script. Workaround: None. |
| 718-SON: Missing error message for invalid nodes in expressions on <code>.PRINT</code> lines | If an invalid node is specified on a Xyce <code>.PRINT TRAN</code> line then Xyce should return a fatal error during netlist parsing (e.g., <code>.PRINT TRAN V(BOGONODE)</code> will produce an error message of undefined symbol in <code>.PRINT</code> command: node BOGONODE, if BOGONODE does not exist in the netlist). However, if the invalid node is inside a Xyce expression (e.g., <code>.PRINT TRAN {V(BOGONODE)}</code>) then Xyce will not produce an error message during netlist parsing and the output value for <code>{V(BOGONODE)}</code> will be zero for all time-steps. Workaround: There is none, other than noticing that an output waveform value is unexpectedly all zeroes, and correcting the <code>.PRINT</code> statement. |
| 715-SON: <code>I(*)</code> for subcircuit nodes does not work properly on <code>.PRINT</code> lines | <code>.PRINT TRAN I(*)</code> works for nodes at the top-level of the netlist. However, it will fail during netlist parsing if there are nodes in subcircuits. The error message will be something like <code>Function or variable I(V:X1:1) is not defined.</code> Workaround: Explicitly put the desired lead or branch currents, using the fully qualified device names, in the <code>.PRINT</code> statement. |
| 707-SON: Behavior for invalid nodes on <code>.FOUR</code> lines and in <code>.MEASURE</code> statements | There are issues with <code>.FOUR</code> lines and <code>.MEASURE</code> statements that accidentally use node names that are not in the netlist. In that case, the <code>.cir.four</code> output file will contain a mix of all zero’s and NaN’s, and Xyce will not produce a warning or error message about the invalid node name. Similarly, the measure statement will run without a warning message about the invalid node name. The measure result will then be zero, rather than FAILED. |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|---|
| <p>661-SON Branch Currents and Power Accessors (I(), P() and W()) Do Not Work Properly in .RESULT Statements</p> | <p>There are two issues. First, .RESULT statements will fail netlist parsing if the requested branch current is omitted from the .PRINT TRAN line. As an example, this statement (.RESULT I(R1)) requires either I(R1), P(R1) or W(R1) to be on the .PRINT TRAN line. Second, the output value, in the .res file, for the lead current or power calculation will always be zero.</p> |
| <p>652-SON: HB output is buggy</p> | <p>While a straightforward use of .print HB works as described in the users and reference guides, several of the documented features do not work as intended. .print HB_FD and .print HB_TD are intended as a way of specifying variable lists for frequency- and time-domain outputs, respectively. It has been discovered that these only produce output if there are print specifications for <i>both</i> frequency and time domain. That is, if only one of .print HB_FD or .print HB_TD is present in the netlist, no output will be produced at all. Workaround: When performing harmonic balance analysis, always specify enough print lines so that both time- and frequency-domain variables are output. This could be by specifying .print HB alone, by specifying both .print HB and .print HB_TD, or by specifying both .print HB_FD and .print HB_TD.</p> |
| <p>583-SON: Switch with RON=0 leads to convergence failure.</p> | <p>The switch device does not prevent a user from specifying RON=0 in its model, but then takes the inverse of this value to get the “on” conductance. The resulting invalid division will either lead to a division by zero error on platforms that throw such errors, or produce a conductance with “Not A Number” or “Infinity” as value. This will lead to a convergence failure. Workaround: Do not specify an identically zero resistance for the switch’s “on” value. A small value of resistance such as 1e-15 or smaller will generally work well as a substitute.</p> |
| <p>469-SON: Belos memory consumption on FreeBSD and excessive CPU on other platforms</p> | <p>Memory or thread bloat can result when using multithreaded dense linear algebra libraries, which are employed by Belos. If this situation is observed, either build Xyce with a serial dense linear algebra library or use environment variables to control the number of spawned threads in a multithreaded library.</p> |
| <p>468-SON: It should be legal to have two model cards with the same model name, but different model types.</p> | <p>SPICE3F5 and ngspice only require that model cards of the same type have unique model names. They accept model cards of different types with the same name. Xyce requires that all model card names be unique.</p> |
| <p>250-SON: NODESET in Xyce is not equivalent to NODESET in SPICE</p> | <p>As currently implemented, .NODESET applies the initial conditions given throughout a full nonlinear solve for the operating point, then uses the result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to a Xyce .NODESET failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround.</p> |
| <p>247-SON: Expressions don’t work on .options lines</p> | <p>Expressions enclosed in braces ({ }) are handled specially throughout Xyce, and may only be used in certain contexts such as in device model or instance parameters or on .PRINT lines.</p> |

Table 3: Known Defects and Workarounds.

| Defect | Description |
|---|--|
| <p>49-SON Xyce BSIM models recognize the model TNOM, but not the instance TNOM</p> | <p>Some simulators allow the model parameter TNOM of BSIM devices to be specified on the instance line, overriding the model parameter TNOM. Xyce does not support this.</p> |
| <p>37-SON: Connectivity checking is broken for devices with more than 10 leads</p> | <p>The diagnostic code used by the Xyce setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If your circuit has that type of large, highly-connected mutual inductor and the code exits with an error message, this bug may be the source of the problem. The error message now includes a recommendation to use the workaround below.</p> <p>Workaround: Disable connectivity checking by adding the line</p> <pre>.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0</pre> <p>to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.</p> |
| <p>27-SON: Fix handling of .options parameters</p> | <p>When specifying .options for a particular package, what gets applied as the non-specified default options might change.</p> |
| <p>1962-SRN: Voltages from interface nodes for subcircuits may not work correctly in expressions on .PRINT lines</p> | <p>An expression that uses a voltage from an interface node to a subcircuit on a .PRINT line may only work if that voltage node is also used outside of the expression on the .PRINT line. A simple example is as follows. The expression $\{V(X1:a)*I(X1:R1)\}$ prints out as 0, unless $V(X1:a)$ is also on the .PRINT line.</p> |
| <p>1923-SRN: LC lines run out of memory, even if equivalent (larger) RLC lines do not.</p> | <p>In some cases, circuits that run fine using an RLC approximation for a transmission line, exit with an out-of-memory error if the (supposedly smaller) LC approximation is used.</p> |
| <p>1595-SRN: Xyce won't allow access to inductors within subcircuits for mutual inductors external to subcircuits</p> | <p>It is not possible to have a mutual inductor outside of a subcircuit couple to inductors in a subcircuit.</p> <p>Workaround: Put all inductors and mutual inductance lines that couple to them together at the same level of circuit hierarchy.</p> |

Supported Platforms

Certified Support

The following platforms have been subject to certification testing for the **Xyce** version 6.8 release.

- Red Hat Enterprise Linux[®] 7, x86-64 (serial and parallel)
- Red Hat Enterprise Linux[®] 6, x86-64 (serial and parallel)
- Microsoft Windows 10[®], x86-64 (serial)
- Apple[®] OS X Sierra, x86-64 (serial and parallel)

Build Support

Though not certified platforms, **Xyce** has been known to run on the following systems.

- FreeBSD 10.x on Intel x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux 6
- Microsoft Windows under Cygwin and MinGW.

Xyce Release 6.8 Documentation

The following **Xyce** documentation is available on the **Xyce** website in pdf form.

- **Xyce** Version 6.8 Release Notes (this document)
- **Xyce** Users' Guide, Version 6.8
- **Xyce** Reference Guide, Version 6.8
- **Xyce** Mathematical Formulation
- Power Grid Modeling with **Xyce**
- Application Node: Using Open Source Schematic Capture Tools with **Xyce**

Also included at the **Xyce** website as web pages are the following.

- Frequently Asked Questions
- Building Guide (instructions for building **Xyce** from the source code)
- Running the **Xyce** Regression Test Suite
- **Xyce**/ADMS Users' Guide
- Tutorial: Adding a new compact model to **Xyce**

External User Resources

- Website: <http://xyce.sandia.gov>
- Google Groups discussion forum: <https://groups.google.com/forum/#!forum/xyce-users>
- Email support: xyce@sandia.gov
- Address:
Electrical Models and Simulation Department,
Sandia National Laboratories
P.O. Box 5800, M.S. 1177
Albuquerque, NM 87185-1177

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.