SANDIA REPORT

SAND2013-7298
Unlimited Release
Printed August 2013

Xyce™ Parallel Electronic Simulator Release Notes Release 6.0

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Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://xyce.sandia.gov/.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 6.0.

Supported Platforms (Certified Support)

Xyce 6.0 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 6.0 release.

- Red Hat Enterprise Linux® 5, x86 (serial only) and x86-64 (serial and parallel)
- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X, x86-64 (serial and parallel)
- TLCC (serial and parallel)
- Red Sky (serial and parallel)

Build Supported Platforms (not Certified)

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 6.0 release. Despite this lack of testing rigor, **Xyce** has been known to run under these configurations.

- FreeBSD 9.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux
- Microsoft Windows under Cygwin and MinGW.

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The **Xyce** team has not determined a minimum memory or processor speed requirement. Any modern computer should have enough memory and processor power to run moderately sized circuits in serial with **Xyce**. Naturally, memory requirements grow with problem size.

Running **Xyce** in parallel will require a system with at least two processors. For problems of the size where parallel operation is beneficial (thousands of devices per processor), one can expect to need several gigabytes of memory per processor.

For the very largest problems that **Xyce** can run (millions of devices), one will require a cluster system with a sufficient number of nodes to distribute the problem efficiently, and sufficient memory per node to support the distributed problem.

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the **Xyce** binary have no run-time software requirements, as they ship with all the shared libraries they need. However, parallel versions require the following software at run time:

- Open MPI (http://www.open-mpi.org/) (version 1.4 or higher)
- TLCC and Red Sky users can load the **xyce** module to properly set the environment

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 11.2.4 (Sandia, http://trilinos.sandia.gov) . This is a suite of libraries including Amesos, AztecOO, Belos, Teuchos, Epetra, EpetraExt, Ifpack, NOX, LOCA, Sacado, Zoltan.

- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (http://www.cise.ufl.edu/research/sparse/umfpack/). This may be provided by the SuiteSparse package that is available on many systems.
- LAPACK
- BLAS

For parallel builds, the following libraries are additionally required:

- Open MPI (http://www.open-mpi.org) library for message passing (version 1.4 or higher). The version used to build Xyce must be the same that is used for building Trilinos.
- ParMETIS (http://glaros.dtc.umn.edu/gkhome/views/metis) library for graph partitioning (version 3.1 or higher). The MPI compiler used to compile ParMETIS must be the same that is used for Trilinos and Xyce.

Xyce Release 6.0 Documentation

The following **Xyce** documentation is available at the **Xyce** website in pdf form.

- **Xyce** Release Notes, Version 6.0
- **Xyce** Users' Guide, Version 6.0
- **Xyce** Reference Guide, Version 6.0
- **Xyce** Building Guide, Version 6.0
- **Xyce** Theory Document
- EKV MOSFET version 3.0.1 model documentation.

New Features and Enhancements

Highlights for **Xyce** Release 6.0 include:

- **Xyce** is being released as open source software under the Gnu Public License, version 3.
- A new variable order Gear time integration method in addition to the existing Trapezoid and BDF integrators.
- Improved support for small-signal frequency domain (.AC) analysis for improved compatibility with SPICE and related analog circuit simulation tools.
- Improved support for harmonic balance (.HB) analysis.

- Extended support for .MEASURE that allows post-processing of output data, including Fourier analysis post-processing.
- A SPICE3F5-compatible lossy transmission line model has been added.
- Direct and adjoint sensitivities are now available for DC calculations.

For details of each of these new features, see the **Xyce** Users' Guide, the **Xyce** Installation Guide, and the **Xyce** Reference Guide. Also, a more complete listing of new features and improvements are given in the following sections.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 6.0.

Table 1: Devices Supported by Xyce

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSPICE enhancements
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model, version 1.2
Bipolar Junction Transistor (BJT) (Level 23)	FBH (Ferdinand-Braun-Institut für Höchstfrequenztechnik) HBT model, version 2.1 **New!**

Table 1: Devices Supported by Xyce

Device	Comments
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	Spice level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	Spice level 6 MOSFET
MOSFET (Level 9)	BSIM3 model
MOSFET (Level 10)	BSIM SOI model
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 103)	PSP model
MOSFET (Level 301)	EKV model
Transmission Line	Lossless
Transmission Line	Lossy **New!**
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
EXT (Level 1)	External device, used for code coupling and power-node parasitics simulations
OP AMP (Level 1)	Ideal operational amplifier
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
ROM (Level 1)	Reduced-order model device for linear (RLC) circuits

Robustness Improvements

- Solver defaults have been modified for increased robustness of parallel runs with a minimum of user-specified options.

New Devices

- FBH HBT_X (version 2.1) Heterojunction Bipolar Transistor model
- SPICE3F5-compatible lossy transmission line

Enhanced Solver Stability, Performance and Features

- Xyce has been updated to use Trilinos 11.2, which has resulted in significant performance improvements.

Defects of Release 5.3 Fixed in this Release

Table 2: Fixed Defects. Note that we have two different bugzilla systems. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
308-SON: Step analysis has bug in transient	There was a subtle bug in .STEP that was not properly resetting solver parameters for each step. This led to very subtle differences between transient runs inside the step loop and identical transient runs without a step loop.
264-SON: Crashes attempting to print expression with global_param	In prior versions of **Xyce**, printing a global_param in an expression on a .PRINT line would cause Xyce to crash. The bug was fixed and printing such parameters is now supported.
267-SON: .print lines in an include file cause the output file to be named after the included file	In prior releases of **Xyce**, a bug in netlist parsing improperly caused the output file created by a .print line that appeared in an include file to be named after the include file instead of the main netlist file. This was fixed, and now the default name for files created by .print is always based on the name of the top-level netlist file, irrespective of the name of the file where the .print actually occurs.
271-SON: Lines with leading tabs not treated as comments	The SPICE3 netlist format states that lines beginning with white space are to be treated as comments. Xyce was not treating leading tabs as such white space, and was processing such lines. This has been corrected.
263-SON/1871-SRN:Use of PDE devices in parallel hangs **Xyce**	A bug in handling of multiple DCOP phases caused any netlist that contained a PDE device to hang **Xyce** if run in parallel. The issue was fixed, and PDE devices can now safely be used in parallel runs.
266-SON: .AC line error if units specified on frequencies after MEG	An error in the ExtendedString class caused the .AC line (and, as it turns out, .DC lines) not to correctly ignore any units specified after multicharacter scale factors such as MEG, i.e. 100MEGHz was not correctly being treated as equivalent to 100MEG. This was fixed, and all such uses now work correctly.
272-SON: Missing AC output features	In previous versions of **Xyce**, output of AC results was severely limited as compared to SPICE implementations. **Xyce** output from .print AC is now fully functional.
229-SON: User defined functions not resolved on .PRINT lines	Functions defined in .func statements were not properly being resolved when used in expressions on .PRINT lines. This usage is now working.
85-SON: Expressions with parameters invalid in .PRINT lines	Attempting to print a parameter (e.g. a symbol defined in a .PARAM statement) in an expression on a .PRINT line would result in an error message about an undefined parameter. The error has been addressed, and printing of .PARAM parameters in print line expressions now works correctly.

Table 2: Fixed Defects. Note that we have two different bugzilla systems. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
1152-SRN: **Xyce** does not allow device names that match node names	A long standing issue in **Xyce** was that an implementation detail of the topology package forbade a user to have a device name that was the same as a node name. This has now been fixed, and node and device names no longer interfere with each other.
1289-SRN: Output interpolation fails to produce expected, smooth curve	The implementation of lead currents for devices was not done in a way that allowed output of those values to be interpolated in the same manner as the solution would be. Output interpolation is required when using high order time integration scheme or `.options output` statements. Lead currents have been reimplemented in a manner that allows their interpolation, and now these signals can have the correct behavior even when output is interpolated.
1909-SRN: Output of voltage differences V(A,B) broken in parallel	Use of voltage difference syntax (V(A,B) to denote the voltage difference between nodes A and B) has never worked in parallel in any prior version of **Xyce**. Older versions of **Xyce** emitted an error message to inform users that the feature didn't work, but very recent versions mistakenly accepted the syntax and emitted results that could be incorrect depending on how nodes were partitioned across processors. The feature has been carefully debugged and now works correctly in both serial and parallel runs.
1852-SRN: VBIC crashes under certain high current conditions	Lack of guarding of a square root expression's argument and issues with voltage limiting led to misbehavior of the VBIC model under some conditions. Both issues have been addressed, and the VBIC model is more robust.
695-SRN: .STEP and .DC sometimes skip final iteration	Roundoff error in an expression used to compute what steps to take sometimes caused the final requested step of a .STEP or .DC loop to be omitted. This has been corrected, and **Xyce** now always runs all requested steps of such sweeps.
291 and 618-SRN: Unclean handling of very small circuits in parallel	The parallel processing features of **Xyce** have always been intended to address very large problems. Early versions of **Xyce** did not always handle very small problems gracefully when run in parallel. The code now examines problem size and is able to run very small circuits in parallel mode. Doing so is almost never beneficial, but the code will let you do it without crashing.
1902-SRN: Harmonic balance crashes if too many frequencies requested	Memory allocation issues involving very large requests have been resolved.

Table 2: Fixed Defects. Note that we have two different bugzilla systems. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
1130-SRN: Parallel version of Xyce cannot run on a single processor	Builds of **Xyce** that were built to be run in parallel were previously unable to be run in serial mode. They are now able to be run both in serial and parallel mode. For routine serial runs, a serial build is preferrable, but parallel builds can now be pressed into serial service if needed.
438-SRN: Output B-H loops from the print line.	It is now possible to output the magnetic flux density B and magnetic field strength H on the print line. See the mutual-inductor device in the reference guide for detailed information.

Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

Defect	Description
855-SRN: AC and HB analysis do not work in parallel	In this version of **Xyce**, analysis types that require use of block linear algebra classes in Trilinos/Epetra do not work in parallel. The analysis types that use block linear algebra classes are AC and HB. *Workaround:* There is no workaround other than to run all such problems in serial.
37-SON: Connectivity checking is broken for devices with more than 10 leads	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If you have such a large mutual inductor and the code exits with an error message, this bug is the source of the problem. The error message now includes a recommendation to use the workaround below. *Workaround:* Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
`.DC` sweep output.	`.DC` sweep calculation does not automatically output the sweep variable. Only variables explicitly listed on the `.PRINT` line are output. *Workaround:* List output sweep variable(s) explicitly in the `.PRINT` statement.

Table 3: Known Defects and Workarounds.

Defect	Description
772-SRN: Infinite-slope transitions in B-sources causes ”time step too small” errors	The nonlinear dependent source (“B-source”) allows the user to specify expressions that could have infinite-slope transitions, such as `Bcrtl OUTA 0 V={ IF( (V(IN) > 3.5), 5, 0 ) }` This can lead to “timestep too small” errors when **Xyce** reaches the transition point. Infinite-slope transitions in expressions dependent only on the `time` variable are a special case, because **Xyce** can detect that they are going to happen in the future and set a “breakpoint” to capture them. Infinite-slope transitions depending on other solution variables cannot be predicted in advance, and cause the time integrator to scale back the timestep repeatedly in an attempt to capture the feature until the timestep is too small to continue. *Workaround:* Do not use step-function or other infinite-slope transitions dependent on variables other than `time`. Smooth the transition so that it is more easily integrated through.

Incompatibilities With Other Circuit Simulators

Table 4: Incompatibilities with other circuit simulators.

Issue	Comment
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the `.TRAN` line.
Mutual Inductor Model.	Not the same as PSpice. This is a Jiles-Atherton non-linear model developed at Sandia. It is compatible with Cadence PSpice parameter set.
`.PRINT` line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work.
BSIM3 level.	In **Xyce** the BSIM3 is MOSEFET level 9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In **Xyce** the BSIM SOI (v3.2) is MOSFET level 10. Other simulators have different levels for the BSIM SOI.
BSIM4 level.	In **Xyce** the BSIM4 is MOSFET levels 14 and 54. Other simulators have different levels for the BSIM4.
Interactive mode.	**Xyce** does not have an interactive mode.
Syntax for `.STEP` is different.	The manner of specifying a model parameter to be swept is slightly different than in some other simulators. See the Users' and Reference Guides for details.
Switch is not the same as SPICE.	The **Xyce** switches are not compatible with the simple switch implementation in SPICE3F5. The switch in **Xyce** smoothly transitions between the ON and OFF resistances over a small range between the ON and OFF values of the control signal (voltage, current, or control expression). See the Reference Guide for the precise equations that are used to compute the switch resistance from the control signal values. The SPICE3F5 switch has a single switching threshold voltage or current, and RON is used above threshold while ROFF is used below threshold. **Xyce**'s switch is considerably less likely to cause transient simulation failures. Results similar to SPICE3F5 can be obtained by setting VON and VOFF to the same threshold value, but this is not a recommended practice.

Important Changes to **Xyce** Usage Since the Release 5.3.

Table 5 lists some usage changes for **Xyce**.

Table 5: Changes to netlist specification since the last release.

Issue	Comment
Time integrator method strings	In all prior versions of **Xyce**, the time integration method was specified using a numeric value, as in `.OPTIONS TIMEINT METHOD=6`. This is still accepted, but **Xyce** now also accepts the more readable specification by strings, e.g. `.OPTIONS TIMEINT METHOD=TRAP`.

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Xyce's expression library is based on that inside Spice 3F5 developed by the EECS Department at the University of California.

The EKV3 MOSFET model was developed by the EKV Team of the Electronics Laboratory-TUC of the Technical University of Crete.

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