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Xyce™ Parallel Electronic Simulator Release Notes Release 6.0.1

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Abstract

The highlights of the *Xyce*™ 6.0.1 release are documented.

Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://xyce.sandia.gov/.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 6.0.1.

Supported Platforms (Certified Support)

Xyce 6.0.1 currently supports any of the following operating system platforms (all versions imply the earliest supported – **Xyce** generally works on later versions as well). These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 6.0.1 release.

- Red Hat Enterprise Linux® 5, x86 (serial only) and x86-64 (serial and parallel)
- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X, x86-64 (serial and parallel)
- TLCC (serial and parallel)
- Red Sky (serial and parallel)

Build Supported Platforms (not Certified)

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 6.0.1 release. Despite this lack of testing rigor, **Xyce** has been known to run under these configurations.

- FreeBSD 9.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux
- Microsoft Windows under Cygwin and MinGW.

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The **Xyce** team has not determined a minimum memory or processor speed requirement. Any modern computer should have enough memory and processor power to run moderately sized circuits in serial with **Xyce**. Naturally, memory requirements grow with problem size.

Running **Xyce** in parallel will require a system with at least two processors. For problems of the size where parallel operation is beneficial (thousands of devices per processor), one can expect to need several gigabytes of memory per processor.

For the very largest problems that **Xyce** can run (millions of devices), one will require a cluster system with a sufficient number of nodes to distribute the problem efficiently, and sufficient memory per node to support the distributed problem.

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the **Xyce** binary have no run-time software requirements, as they ship with all the shared libraries they need. However, parallel versions require the following software at run time:

- Open MPI (http://www.open-mpi.org/) (version 1.4 or higher)
- TLCC and Red Sky users can load the **xyce** module to properly set the environment

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 11.2.4 (Sandia, http://trilinos.sandia.gov) . This is a suite of libraries including Amesos, AztecOO, Belos, Teuchos, Epetra, EpetraExt, Ifpack, NOX, LOCA, Sacado, Zoltan.

- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (http://www.cise.ufl.edu/research/sparse/umfpack/). This may be provided by the SuiteSparse package that is available on many systems.
- LAPACK
- BLAS

For parallel builds, the following libraries are additionally required:

- Open MPI (http://www.open-mpi.org) library for message passing (version 1.4 or higher). The version used to build Xyce must be the same that is used for building Trilinos.
- ParMETIS (http://glaros.dtc.umn.edu/gkhome/views/metis) library for graph partitioning (version 3.1 or higher). The MPI compiler used to compile ParMETIS must be the same that is used for Trilinos and Xyce.

Xyce Release 6.0.1 Documentation

The following **Xyce** documentation is available at the **Xyce** website in pdf form.

- **Xyce** Release Notes, Version 6.0.1
- **Xyce** Users' Guide, Version 6.0.1
- **Xyce** Reference Guide, Version 6.0.1
- **Xyce** Building Guide, Version 6.0.1
- **Xyce** Theory Document
- EKV MOSFET version 3.0.1 model documentation.

New Features and Enhancements

Highlights for **Xyce** Release 6.0.1 include:

- Numerous bug fixes (see Table 2)
- New initial guess option for HB analysis

For details of each of these new features, see the **Xyce** Users' Guide, the **Xyce** Installation Guide, and the **Xyce** Reference Guide. Also, a more complete listing of new features and improvements are given in the following sections.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 6.0.1.

Table 1: Devices Supported by Xyce

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSPICE enhancements
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model, version 1.2
Bipolar Junction Transistor (BJT) (Level 23)	FBH (Ferdinand-Braun-Institut für Höchstfrequenztechnik) HBT model, version 2.1
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	Spice level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	Spice level 6 MOSFET

Table 1: Devices Supported by Xyce

Device	Comments
MOSFET (Level 9)	BSIM3 model
MOSFET (Level 10)	BSIM SOI model
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 103)	PSP model
MOSFET (Level 301)	EKV model
Transmission Line	Lossless
Transmission Line	Lossy
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
EXT (Level 1)	External device, used for code coupling and power-node parasitics simulations
OP AMP (Level 1)	Ideal operational amplifier
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
ROM (Level 1)	Reduced-order model device for linear (RLC) circuits

Defects of Release 6.0 Fixed in this Release

Table 2: Fixed Defects. Note that we have two different bugzilla systems. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
BUG 434-SON: Xyce crashes when built with Clang version 3.3 or higher	A number of functions that should have returned values were not doing so. This is a fatal error with clang versions 3.3 and higher. The offending functions now return appropriate values.
BUG 436-SON: .options output selction of output times after initial interval does not work	Selection of output intervals as described in section 9.2 of the Users Guide did not work as advertised. The "initial_interval" was used for all time, and additional time/interval pairs were being ignored. The defect was corrected, and the code performs as the manual says it should.
BUG 379-SON: sdt() function on print line does not work	Using the sdt (time integration) function in an expression on a .print line produced incorrect results. This has been fixed.
BUGs 381, 419, 421, 423, 424-SON: numerous errors in tecplot output for HB, homotopy, and .step	Tecplot output of certain types of runs was not correct, and the errors have been corrected.
BUG 433-SON: error in transient assisted HB initial guess calculation	During the calculation of the initial guess for harmonic balance analysis, a transient is run and the number of time steps is used to determine a good tolerance to run the transient analysis. However, the wrong function was being called to find the number of time steps, with the result that tolerances were being repeatedly reduced. The error was corrected.
BUG 1917: Rise/Fall/Delay measure needs a regression test.	The `.measure` function `TRIG=, TARG=` was not tested and did not work correctly. This has been fixed.
BUG 1918: measure freq needs to support FROM, TO qualifier.	The `.measure` function `freq` now supports the use of `FROM` and `TO` to specify a time range for the measurement.

Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

Defect	Description
`.DC` sweep output.	`.DC` sweep calculation does not automatically output the sweep variable. Only variables explicitly listed on the `.PRINT` line are output. *Workaround:* List output sweep variable(s) explicitly in the `.PRINT` statement.
27-SON: Fix handling of .options parameters	When specifying .options for a particular package, what gets applied as the non-specified default options might change.
37-SON: Connectivity checking is broken for devices with more than 10 leads	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If you have such a large mutual inductor and the code exits with an error message, this bug is the source of the problem. The error message now includes a recommendation to use the workaround below. *Workaround:* Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
195-SON: Restart files are not produced if initial_interval is not specified	The users' guide states that if `.OPTIONS RESTART` is specified without an `INITIAL_INTERVAL` that the restart file will be saved at every time step. This is not working, and if no initial interval is specified, no restart is saved at all. *Workaround:* Always specify a suitable initial interval when requesting restart.
244-SON: The defaults in Xyce bsimsoi do not match defaults in spice3 bsimsoi	Some of the default parameters used in the BSIM3 SOI (level 10) MOSFET do not match SPICE3F5's defaults, leading to observed differences in behavior if a model card does not specify these parameters. *Workaround:* The parameters at issue appear all to be parameters that have *computed* rather than hard-coded defaults. These include `CGDO`, `CGSO`, `K1`, `K2`, `XJ`. It is best to use extracted values for these parameters rather than relying on the defaults until this bug is fixed.

Table 3: Known Defects and Workarounds.

Defect	Description
227-SON: Expressions don't work on .options lines	Expressions enclosed in braces ({ }) are handled specially throughout Xyce, and may only be used in certain contexts such as in device model or instance parameters or on `.PRINT` lines.
250-SON: NODESET in xyce is not equivalent to NODESET in spice	As currently implemented, .NODESET applies the initial conditions given throughout a full nonlinear solve for the operating point, then uses the result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to Xyce's .NODESET failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround.
365-SON: Missing Default Instance Length Parameter in Resistor Model Parameters	The resistor allows a semiconductor resistor formulation given a sheet resistance, length, and width, but no reasonable default is given for the length. A default width parameter is provided through the model card, and is used if no width is specified on the instance line. *Workaround:* Always specify a length on the instance line for any resistor for which the semiconductor resistor syntax is used (see reference guide for usage).
384-SON: Errors compiling with Bison 3.0	Bison 3.0's C++ parser has changed significantly and thus Bison version 3.0 cannot be used to build Xyce's reaction parser. *Workaround:* Use only Bison versions between 2.3 and 2.7 if reaction parser is desired. Disable building of the reaction parser by configuring with `--disable-reaction_parser` if unable to provide a suitable version of Bison.
387-SON: Failure to find <file> in .lib <file> causes Xyce to emit confusing error message	If a `.LIB` statement is given a file argument, but the file cannot be found, an error in input processing causes Xyce to exit with an error stating that no analysis statement was specified instead of a more meaningful "cannot find file" error.
401-SON: Frequency-domain-specific voltage drop specifiers produce incorrect output	The VR, VI, VM, VP and VDB output specifiers for printing real and imaginary parts, magnitude, phase, or magnitude in DB of voltages in frequency domain do not work if given two nodes, but Xyce will not emit any warning or error messages. *Workaround:* Unfortunately there is no workaround to this bug, because in Xyce 6.0.1 the VR, VI, VM, VP and VDB functions don't work inside expressions, either. Both bugs are fixed in code targeted for the 6.1 release.
412-SON: .measure ... when ... cross= does not seem to work as advertised	The code to process the .measure ... when... cross=... construct is not working correctly. There is no work-around.

Table 3: Known Defects and Workarounds.

Defect	Description
413-SON: parser ignores instance parameters if user incorrectly places them before model name	If instance parameters (e.g. length or width of a MOSFET device) are placed before the model name on an instance line, Xyce simply ignores them without emitting a syntax error message. *Workaround:* Place all instance parameters at the end of an instance line after the model name. Place nothing between the node list and the model name.
427-SON: Certain subcircuit nodes cannot be accessed in expressions	Xyce allows nodes within a subcircuit to be referenced in expressions and on .print lines using the syntax "<subcircuit instance name>:<nodename>". On .print lines this works even if the node named is one that is on the subcircuit declaration line (i.e., dummy argument nodes, which are just aliases for names in the calling circuit context). This does not work inside expressions. *Workaround:* Use the name of the node at the higher level of the circuit instead of the dummy argument names.
772-SRN: Infinite-slope transitions in B-sources causes "time step too small" errors	The nonlinear dependent source ("B-source") allows the user to specify expressions that could have infinite-slope transitions, such as `Bcrtl OUTA 0 V={ IF( (V(IN) > 3.5), 5, 0 ) }` This can lead to "timestep too small" errors when **Xyce** reaches the transition point. Infinite-slope transitions in expressions dependent only on the `time` variable are a special case, because **Xyce** can detect that they are going to happen in the future and set a "breakpoint" to capture them. Infinite-slope transitions depending on other solution variables cannot be predicted in advance, and cause the time integrator to scale back the timestep repeatedly in an attempt to capture the feature until the timestep is too small to continue. *Workaround:* Do not use step-function or other infinite-slope transitions dependent on variables other than `time`. Smooth the transition so that it is more easily integrated through.
855-SRN: AC and HB analysis do not work in parallel	In this version of **Xyce**, analysis types that require use of block linear algebra classes in Trilinos/Epetra do not work in parallel. The analysis types that use block linear algebra classes are AC and HB. *Workaround:* There is no workaround other than to run all such problems in serial.
1595-SRN: Xyce won't allow access to inductors within subcircuits for mutual inductors external to subcircuits	It is not possible to have a mutual inductor outside of a subcircuit couple inductors in a subcircuit. *Workaround:* Put all inductors and mutual inductance lines that couple them together at the same level of circuit hierarchy.

Table 3: Known Defects and Workarounds.

Defect	Description
1922-SRN: Xyce nonlinear core model defaults seriously underestimate hysteresis effects for small signals	The magnetic core model has some parameter defaults that effectively turn off magnetic effects when small-amplitude driving signals are applied. This can show up when attempting to generate B-H loops for magnetic cores using standard test harnesses. A robust solution to this issue is being sought. *Workaround:* Set the two parameters DELV and VINF so that the ratio DEVLV/VINF is as high as possible without causing convergence problems. Ratios as high as 1e6 are appropriate. Unfortunately, ratios this large can begin to cause convergence problems when high-amplitude signals are applied.

Incompatibilities With Other Circuit Simulators

Table 4: Incompatibilities with other circuit simulators.

Issue	Comment
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the `.TRAN` line.
Mutual Inductor Model.	Not the same as PSpice. This is a Jiles-Atherton non-linear model developed at Sandia. It is compatible with Cadence PSpice parameter set.
`.PRINT` line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work.
BSIM3 level.	In **Xyce** the BSIM3 is MOSEFET level 9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In **Xyce** the BSIM SOI (v3.2) is MOSFET level 10. Other simulators have different levels for the BSIM SOI.
BSIM4 level.	In **Xyce** the BSIM4 is MOSFET levels 14 and 54. Other simulators have different levels for the BSIM4.
Interactive mode.	**Xyce** does not have an interactive mode.
Syntax for `.STEP` is different.	The manner of specifying a model parameter to be swept is slightly different than in some other simulators. See the Users' and Reference Guides for details.
Switch is not the same as SPICE.	The **Xyce** switches are not compatible with the simple switch implementation in SPICE3F5. The switch in **Xyce** smoothly transitions between the ON and OFF resistances over a small range between the ON and OFF values of the control signal (voltage, current, or control expression). See the Reference Guide for the precise equations that are used to compute the switch resistance from the control signal values. The SPICE3F5 switch has a single switching threshold voltage or current, and RON is used above threshold while ROFF is used below threshold. **Xyce**'s switch is considerably less likely to cause transient simulation failures. Results similar to SPICE3F5 can be obtained by setting VON and VOFF to the same threshold value, but this is not a recommended practice.

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Xyce's expression library is based on that inside Spice 3F5 developed by the EECS Department at the University of California.

The EKV3 MOSFET model was developed by the EKV Team of the Electronics Laboratory-TUC of the Technical University of Crete.

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