Xyce™ Parallel Electronic Simulator
Version 6.4 Release Notes

Sandia National Laboratories

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The ***Xyce***™ Parallel Electronic Simulator has been written to support the simulation needs of Sandia National Laboratories' electrical designers. ***Xyce***™ is a SPICE-compatible simulator with the ability to solve extremely large circuit problems on large-scale parallel computing platforms, but also includes support for most popular parallel and serial computers.

For up-to-date information not available at the time these notes were produced, please visit the ***Xyce***™ web page at `http://xyce.sandia.gov`.

Highlights for the ***Xyce***™ 6.4 Release include:

- New devices, such as VBIC 1.3, MEXTRAM with self-heating, and the Yakopcic Memristor
- New Local truncation Error (LTE) criterions for time-step control
- Oversampling capability for Harmonic Balance time domain output
- Last release with full support for Red Hat Linux 5

Contents

New Features and Enhancements

New Devices and Device Model Improvements

- VBIC version 1.3, 3- and 4-terminal variants (Q levels 11 and 12)
- MEXTRAM 504.11 with self-heating (Q level 505)
- A new memristor device using the Yakopcic model
- Support for Reactive Power limits in the Power Grid Generator Bus model.
- Improved compatibility between **Xyce** and PSpice Digital Behavioral models.

Enhanced Solver Stability, Performance and Features

- The Kundert SPARSE linear solver has been added as a linear solver option in Xyce.
- The netlist parser has been significantly refactored to reduce memory consumption and improve parsing speeds for large circuits.
- Improved Harmonic Balance (HB) robustness during the initial guess calculation.
- New Local truncation Error (LTE) criterions that use history information of signals improve time stepping for all time integrators.
- Oversampling capability for Harmonic Balance time domain output enables users to produce well-resolved time-domain outputs.
- Arclength continuation is now much more useful and robust.
- Sensitivity analysis can now allow multiple objective functions.

Interface Improvements

- Power calculations supported for controlled-source devices (B,E,F,G and H).
- Support for additional .MEASURE statement syntaxes.
- New output options, that allow the user to suppress the header and footer of standard-format output files.
- Improved error handling during netlist parsing.
- Improved Harmonic Balance Output.
- New support for the DIGINITSTATE option, which sets the initial state of the Digital Flip-Flip and Latch devices.

Defects Fixed in this Release

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
302-SON: Support re-measure of existing **Xyce** simulation data	Re-measure was documented in the **Xyce** 6.3 Reference Guide. Subsequent testing showed that re-measure did not work correctly for: a) parallel execution of **Xyce**; or b) when the measure line used an expression. This has been fixed.
308-SON: `.STEP` analysis has a subtle bug for transient simulation	`.STEP` analysis applies an outer parameter stepper loop around another analysis type such as transient. When `.STEP` was applied to transient, the transient output was not identical to the output from equivalent stand-alone transient analyses. This bug was only present in the BDF time integrator. This has been fixed.
414-SON: Fix the nonlinear solver convergence tests to be simpler and make more sense	The nonlinear solver in **Xyce** had an overly-complex set of convergence tests that were not necessary. Occasionally, this complexity would prevent convergence of circuits, or under very rare instances, allow solver failures to be declared as passed. This has been fixed.
440-SON: `.MEASURE` should properly support signals with DC offsets and measures that use resistor lead currents	`.MEASURE` statements did not function correctly if the measured quantity either did not start at 0 at time=0 or used a resistor lead current. Simple examples were measuring the maximum level of the voltage source defined as `VCOS 1 1a SIN(0 5 100K -2.5U)` or measuring the maximum current level through a resistor with `.MEASURE TRAN MAXIR MAX I(RTEST).`
540-SON : **Xyce** incorrectly added extensions to file names specified on print lines	In **Xyce** 6.2, the behavior of the `FILE=` option to `.PRINT` lines was inadvertently changed. In versions 6.2 and 6.3, the code incorrectly added format-specific extensions to the file name specified, e.g. `FILE=myfile` would actually result in a file called `myfile.prn` for the standard output format. This was not intended, and was reported by users too soon before the 6.3 release to be corrected in that release. **Xyce** 6.4 does not add this undesired extension, and the file name specified is once again used exactly as specified. **NOTE:** The file name specified by `FILE=` is used only for the primary output file associated with the print line. For print lines that result in multiple output files the secondary outputs are still given default file names based on the netlist name and output format. As an example, if the input file is called "netlist.cir", `.print HB FILE=a` will output the primary data (frequency-domain solution) to the file "a", but the secondary data (time-domain solution) to "netlist.cir.HB.TD.prn" rather than using the file name specified as a base name. **This choice of file name for secondary outputs may change in future releases.** Additional `.PRINT` options exist to specify file names for these secondary outputs, such as `.print HB_TD FILE=b` to output the time domain data to file "b".
554-SON: PDE_1D_BJT/gilbert_cell_pde_four test failing on parallel RHEL5 since mid-October	The "gilbert_cell_pde_four" test was failing on Windows and RHEL5 builds at various times prior to the release of **Xyce** 6.3. The problem was with the test circuit not having tight enough tolerances, so it had variable results. The tolerances were tightened and the failures stopped.

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Defect	Description
573-SON: Continuation does not work in HB solves	Prior to **Xyce** 6.3, specification of LOCA continuation options in `.OPTIONS NONLIN-HB` would be accepted but continuation would not actually be applied. This was fixed in **Xyce** 6.3, but had not been documented in the 6.3 Release Notes.
592-SON: Make `.IC` and `.NODESET` be able to use expressions	In **Xyce** 6.3, if one attempted to use expressions on the `.IC` line, the simulation would fail, as the code was not instrumented to handle this properly. The same was true for `.NODESET`. This has been fixed for **Xyce** 6.4.
606-SON and 654-SON: Make TEMP and Vt work correctly in B source expressions	It was observed that if a B source expression used the TEMP variable, the value of the expression was not correctly being updated if TEMP was swept in a `.STEP` loop. Furthermore, the **Xyce** documentation has always stated that Vt is a reserved variable name, but **Xyce** neither defined the Vt variable nor allowed it to be used in B source expressions. Release 6.4 fixes both of these issues, allowing TEMP and Vt to be used in B source expressions, and correctly updating them in `.STEP` loops.
614-SON: PDE (TCAD) Device nonlinear Poisson initialization needs to work properly with LOCA	Prior to **Xyce** 6.3, specification of LOCA continuation in `.OPTIONS NONLIN` for a PDE(TCAD) problem would lead to a logic error that often resulted in nonconvergence. The TCAD devices by default solve a nonlinear Poisson problem first, followed by the full drift-diffusion formulation at the DCOP. The nonlinear Poisson calculation can be manually turned off, but typically is not, as it provides a good initial guess. The logic error was that if running a continuation loop, the nonlinear Poisson calculation would be re-computed at each step of the continuation, and it only should have been computed for the very first step. This has been fixed for **Xyce** 6.4.
624-SON: GMIN stepping output gets put into TRAN output file under some circumstances	This issue happened when the user specified an output filename on the `.PRINT` line. **Xyce** would incorrectly use that filename for all the outputs, even if it had only been specified for one type of analysis (such as transient). When this happened, output that should have been in separate files was all concatenated into the same file. This was not the intended behavior, and it has been fixed in **Xyce** 6.4. For example, if the user specifies a output file name for the transient `.PRINT` line, the resulting file with this name will only contain transient output. Other outputs, such as output for GMIN stepping will be directed to a separate file using the default filename for that analysis type.
629-SON: Power accessors (P() and W()) do not work in expressions	P() and W() now work in expressions in both top-level circuits and subcircuits.

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Defect	Description
632-SON: Fix LOCA interface so that we can use arclength continuation with voltage limiting on	Arclength continuation only worked if voltage limiting was turned off by setting `.options device voltlim=0`. This was because the arclength equation was required the sensitivity of the system with respect to the continuation parameter. This was computed using a finite-difference calculation, that conflicted with voltage limiting. This issue has been fixed in **Xyce** 6.4. Many devices are now instrumented to provide analytic parameter sensitivities to support `.SENS`. The interface to LOCA has been refactored to use these sensitivities when available. When not available, a new finite-difference has been implemented that temporarily disables voltage limiting.
636-SON: **Xyce** core dumps on invalid `.TRAN` line	A `.TRAN` line with only one of the two required arguments caused **Xyce** versions 6.1 through 6.3 to crash with a core dump. This error was fixed in **Xyce** 6.4.
641-SON: Core Dumps Caused by OBJFUNC Contents in .SENS	This occurred if an invalid objective function was specified for a sensitivity analysis. For example, sensitivity analysis objective functions currently cannot process output functions such as the power accessors, so a specification such as `.SENS objfunc=P(R1)` would cause a core dump in **Xyce** 6.3. This has been fixed for **Xyce** 6.4.
644-SON: Wrong number of arguments on .DC line causes segfault	This line (`.DC V1 -8.0 -4.0 0.0 4.0`) would cause a core dump, since the last 4.0 is extraneous. Incorrect .DC lines should now produce useful error messages and graceful exits.
646-SON: .csd format for PROBE output is incorrect for specific numbers of output variables	This line (`.PRINT TRAN FORMAT=PROBE V(1) V(2) V(3) V(4)`) would produce an incorrectly formatted .csd file that would not open in PSpice. In general, the bug occurred if the number of output variables (N) on the `FORMAT=PROBE` print line satisfied this equation: (N+1)mod5 = 0. It works correctly now.
647-SON : Instance parameters copied from model at wrong time, breaking step loops	Some devices have default values of instance parameters that are computed from model parameters. If a device is instantiated without specifying these instance parameters, the default is computed and used. In versions of **Xyce** prior to 6.4, this computation was performed once, when the device was first created. This is incorrect if any of the model parameters used in the computation are being varied in a `.STEP` loop. In such a case, the instance parameter would not properly be updated as the model parameter was varied. This has been fixed in **Xyce** 6.4 for all devices that had the problem, which included most MOSFET devices and all devices that had been generated from Verilog-A sources.
648-SON: .print HOMOTOPY doesn't work with .DC or .TRAN	An error trap in the **Xyce** 6.3 parser was too agressive. It was attempting to check that the specified `.print` lines matched the specified analysis lines. As the keyword `HOMOTOPY` didn't match `DC` or `TRAN`, the parser incorrectly threw an error. Continuation methods are often used to compute DC operating points, that are then used as the starting point for a transient analysis. So, it was natural that one might request such output. This has been fixed for **Xyce** 6.4.

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Defect	Description
652-SON (partially) : HB output is buggy	Release 6.3 of **Xyce** had a bug that would garble harmonic balance output if a `FILE` keyword was used on the `.print HB` line to redirect output to a specified file name instead of the default file name. The result was that time- and frequency-domain data were improperly placed on the same line of the same output file, and the output file contained both time- and frequency-domain header lines. This part of bug 652 was resolved: the `FILE` option of the `.print HB` line now redirects only the frequency-domain data, and the time-domain data is sent to the default-named file (the netlist name with a ".HB.TD" suffix and an extension. A further bug in HB output from release 6.3 was fixed, in that the special `.print HB_TD` and `.print HB_FD` output lines may be used as documented in the Reference Guide in order to specify different variables to be printed for time- and frequency-domain harmonic balance output, and to redirect that output to non-default file names with `FILE` keywords. But an unresolved part of this bug means that these options must be used as a pair — **Xyce** 6.4 will not output anything at all if only time- or frequency-domain data is requested. See also the "Known Defects" table for further description of this bug.
657-SON: **Xyce** core dumps during PWL source parsing if the time-voltage pair list is missing	A piecewise linear (PWL) source definition without a list of time-voltage pairs caused a core dump. An example instance line was: `V4 4 0 PWL TD=1 R=1`. This is now fixed.
658-SON : Multiple print lines to same file should work intuitively	In prior releases of **Xyce**, having multiple print lines that output to the same file was not supported, and if attempted would not do what a user would have expected — and the specific behavior observed would depend on which version of **Xyce** was used. The feature has been implemented, and if multiple `.PRINT` lines for the same analysis type are specified that output to the same file, the variable lists of each are aggregated so that the net effect is the same as having a single print line with all the specified variables. Multiple print lines for the same analysis to different files do not aggregate in this manner. Multiple print lines for analyses that result in multiple files, such as `.print HB`, aggregate the variable lists for all the secondary files as well as the primary file. It is an error to attempt to have multiple print lines to the same file with different `FORMAT` specifications.
663-SON: Lead currents for the method=trap integrator have a mistake in the first transient time step	The lead current feature in **Xyce** has undergone numerous internal changes recently. As a result, a bug was introduced into the trapezoid rule integration version of lead currents, which resulted in incorrect lead currents in some circuits, in the initial time step out of the DCOP calculation. Time derivatives should have always been near zero at this phase of the calculation, but this bug caused them to be much larger under some circumstances. This has been fixed.

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Defect	Description
664-SON: Fix the old nonlinear solver's convergence tests to be consistent with the NOX convergence test	This is approximately the same bug as 414-SON (described above). The only difference is that it is applied to the non-default, older nonlinear solver. As with the default solver (NOX), the convergence tests were too complex and occasionally resulted in nonlinear solver failures, or cases where failed solves were declared as passed. This has been fixed for **Xyce** 6.4.
668-SON: **Xyce** Core dumps on some invald .OPTIONS lines	Examples of the offending, incorrect .OPTIONS lines included: `.OPTIONS` and `.OPTIONS LINSOL type=`. This is fixed now.
669-SON: Sensitivity analysis does not recognize default device parameters	If performing sensitivity analysis, it was not possible to use default device parameters. For example, `.sens param=Rtest:R` would work, but `.sens param=Rtest` would not. This is fixed now.
673-SON: Core dumps caused by incomplete `.MEASURE` lines	**Xyce** would core dump on some incomplete `.MEASURE` lines. Examples included: `.MEASURE TRAN` and `.MEASURE`. Another cause was when the `<variable>=<val>` portion of the line was missing, such as `.MEASURE TRAN DERIV1 DERIV`. This is fixed now.
674-SON: HB startup output is broken and HB tecplot output has a bug	The HB startup output contains wrong information. It was the same information as HB IC output. The HB IC output for tecplot format is not correct if the transient analysis needs to be re-run with tighter tolerance during the initial guess calculation. This has been fixed.
675-SON: HB has a bug when the tolerance is tightened during the initial guess calculation	When the transient analysis is re-run with a tighter tolerance during the initial guess calculation, the second transient run could fail at DCOP or after a few steps. However, the equivalent stand-alone transient analysis runs to completion. This has been fixed.
679-SON: TRIG V(A)=V(B) or TARG V(C)=V(D) syntax did not work in `.MEASURE`	The TRIG and TARG clauses did not work correctly if the trig or targ level was a variable level rather than a fixed level (e.g., `TRIG V(A)=V(B) TARG V(C)=0.5`). In this example, the TRIG clause uses a variable level (`V(B)`), while the TARG clause uses a fixed level of 0.5V. This is fixed now.
681-SON : Stepping over BSIM3 and BSIM4 model parameters gives wrong results	The mechanism used in the BSIM3 and BSIM4 to share size-dependent quantities derived from model parameters between several instances of the same size was not set up to work with `.STEP` loops. If the `.STEP` loop was over a BSIM3 or BSIM4 model parameter, the derived quantities would not be updated after the initial computation. This is similar, but not identical, to bug 647-SON, above . The BSIM3 and BSIM4 devices now clear out their saved lists of derived parameters if any model parameters change.
682-SON: "Spice strategy" only attempted on first DC bias point	Since **Xyce** 6.2, **Xyce** will attempt to solve a DC bias point using a three-step strategy: Newton iteration, GMIN-stepping, and source-stepping. This is the same strategy that SPICE 3F5 uses. In **Xyce** 6.2 and **Xyce** 6.3 there was a bug that caused this strategy only to be applied at the first step of a `.DC` sweep. If subsequent points in the sweep failed Newton iteration, no further attempts were made to obtain a solution for those points. This error has been corrected in release 6.4; the strategy will be followed any time a DC bias point is computed.

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Defect	Description
690-SON: Fix various WHEN syntaxes for the DERIV measure	The DERIV measure did not work correctly for some syntaxes in the WHEN clause. This included having a variable as the target level (e.g., `WHEN V(A)=V(B)`). It also included the syntax `DERIV V(A) WHEN V(B)=0.5` if A and B were different. This is fixed now.
694-SON: Core dumps from invalid `.PRINT` lines	Examples of the offending, incorrect `.PRINT` lines included: `.PRINT V(1` and `.PRINT V()`. This is fixed now.
699-SON: Fix core dumps in `.FOUR` and FOURIER measure statements	**Xyce** would core dump on several invalid or poorly chosen `.FOUR` lines and `FOURIER` measure statements. The first was when a negative fundamental frequency was requested, for either `.FOUR` or `.MEASURE`. The second was when the measurement window, for a `.MEASURE` statement, only contained one time point. The last was when a netlist contained multiple `.FOUR` lines. These issues have been fixed.
700-SON: Random number use in level 3 synapse limited to one instance	Random number use within this synapse device has been fixed so that individual instances share the same underlying random number generator, and will get a unique random number each time the generator is called. Thus, they will no longer follow the same sequence of random numbers.
705-SON: Bad argument to `.SAVE` causes **Xyce** to go into an infinite loop	This invalid line (`.SAVE filename=<name>`) would cause **Xyce** to enter an infinite loop during netlist parsing. This is fixed now. The overall error handling and error messages for invalid and ill-formatted `.SAVE` lines were improved.
710-SON: dQdx derivatives in the BSIM3 and BSIM4 devices need to be loaded into the matrix unconditionally	In some devices, the capacitive terms are excluded from the DCOP Jacobian, and also from the Jacobian of the first Newton iteration of the first time step. This was done because the capacitive currents at the DCOP are by definition zero. However, there are use cases (such as using a MOSFET device as a capacitor), where doing it this way caused singular matrices. This has been fixed for **Xyce** 6.4.
1794-SRN: Fix core dump in outputting when the number of devices is less than number of processors	This issue only applies to a parallel build of **Xyce**. If the devices are distributed such that one processor does not have any devices, then the code for outputting data could attempt to access an empty container resulting in a segmentation fault. This issue has been fixed.
1958-SRN: LOCA fails to reset properly after a failed step, for PDE devices	This issue was specific to PDE devices. If attempting to obtain a steady-state solution using a homotopy method, PDE devices were not having their previous state restored after failed steps. As a result, all subsequent attempts at the step would fail, and the steady-state solution would not be obtained. This was due to a logic error in these device models and has been fixed. The issue applied to all PDE devices.

Interface Changes in this Release

Table 2: Changes to netlist specification since the last release.

Change	Detail
.MEASURE output is in scientific notation.	The .MEASURE output, in both the .mt0 file and standard output, is in scientific notation now.
The SIN() transient specification for the V and I devices supports a `PHASE` parameter.	The `PHASE` parameter was supported in past **Xyce** releases but was not documented in the Reference Guide.
Xyce now supports the DIGINITSTATE option.	PSpice supports a DIGINITSTATE option that controls the behavior of latches and flip-flops during the DC Operating Point calculation. This capability is now in **Xyce**, but for backwards compatibility, its default behavior differs from PSpice.
The behavior of a **Xyce** piecewise linear (PWL) source when the time-voltage list omits an entry for time=0.	The **Xyce** behavior in this case now matches PSpice and HSpice. See the V and I device sections of the Reference Guide for more details.
The behavior of `.PRINT HB FILE=` was broken in previous releases.	It was discovered that **Xyce** 6.3 would output both time-domain and frequency-domain data into the same file when the `FILE` option was used on harmonic balance print lines. This was never intended behavior. **Xyce** 6.4 outputs time and frequency domain data to separate files, whether or not the `FILE` option is given. In this release of **Xyce**, the named file is where the frequency-domain data is sent. The time-domain data is sent to a file whose name is the netlist name with the suffix ".HB.FD" followed by an extension determined by the output format. To send the time-domain data to a file with a different name, use the `.print HB_TD FILE=` line *in addition to* either a `.print HB` or `.print HB_FD` line.
In previous releases, **Xyce** treated all lines with leading whitespace as comments.	The **Xyce** behavior now is to treat lines that begin with whitespace as comments UNLESS the first non-whitespace character is a "+", in which case it treats the line as a continuation. This is consistent with how Spice3F5 handles lines with leading whitespace.
Character limit of top-level netlist title line.	In previous releases, **Xyce** limited the first line of any top-level netlist file (the title line) to 256 characters. This limitation has been removed.

Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

Defect	Description
704-SON: Lead currents do not work in AC analyses, crash **Xyce**	Lead currents for devices other than voltage sources are not solution variables, and are computed by **Xyce** as a derived quantity in a post-processing step. This is not set up correctly to work when doing small-signal AC analysis. Attempting to print such a lead current or any of its computed quantities (magnitude, phase, real or imaginary parts) will cause **Xyce** to crash. The lead currents do work as expected in time-domain analysis such as transient and DC. Lead currents work properly in HB frequency-domain analysis. ***Workaround***: Do not attempt to print currents through a device other than a voltage source in any AC simulation. If you need the current through a device under AC analysis, place a zero-volt voltage source in series with that device, and print the current through the voltage source.
703-SON and 698-SON Lead currents and the power accessors do not work consistently in `.FOUR` and `.MEASURE` statements	`.FOUR` and `.MEASURE` statements will fail netlist parsing if the requested branch current is omitted from the `.PRINT TRAN` line. As an example, this statement (`.MEASURE TRAN MAXI MAX I(R1)`) requires either `I(R1)`, `P(R1)` or `W(R1)` to be on the `.PRINT TRAN` line.
702-SON Expressions that use VSRC currents (in B sources or in `.SENS` objfunc specifications) can produce wrong derivatives	As an example, if `VA` is a voltage source, and `B` is a node name then `objfunc={V(B)*V(B)}` will get the right answer but `objfunc={I(VA)*I(VA)}` will get the wrong answer.
657-SON Make `.IC` and `.NODESET` usable inside subcircuits	`.IC` and `.NODESET` statements within subcircuits are silently ignored by **Xyce**. ***Workaround***: The `.IC` and `.NODESET` sections of the **Xyce** Reference Guide describe how to work around this bug by moving the statements to the top-level of the circuit.
652-SON: HB output is buggy	While a straightforward use of `.print HB` works as described in the users and reference guides, several of the documented features do not work as intended. `.print HB_FD` and `.print HB_TD` are intended as a way of specifying variable lists for frequency- and time-domain outputs, respectively. It has been discovered that these only produce output if there are print specifications for *both* frequency and time domain. That is, if only one of `.print HB_FD` or `.print HB_TD` is present in the netlist, no output will be produced at all. This bug was discovered too late to be fixed in time for release 6.4. ***Workaround***: When performing harmonic balance analysis, always specify enough print lines so that both time- and frequency-domain variables are output. This could be by specifing `.print HB` alone, by specifying both `.print HB` and `.print HB_TD`, or by specifying both `.print HB_FD` and `.print HB_TD`.

Table 3: Known Defects and Workarounds.

Defect	Description
583-SON: Switch with RON=0 leads to convergence failure.	The switch device does not prevent a user from specifying `RON=0` in its model, but then takes the inverse of this value to get the "on" conductance. The resulting invalid division will either lead to a division by zero error on platforms that throw such errors, or produce a conductance with "Not A Number" or "Infinity" as value. This will lead to a convergence failure. ***Workaround***: Do not specify an identically zero resistance for the switch's "on" value. A small value of resistance such as 1e-15 or smaller will generally work well as a substitute.
526-SON: The RISE/FALL/CROSS features of `.MEASURE` should work for all measures (where appropriate)	The `LAST` keyword may not work correctly for some measure types and syntaxes.
478-SON: Measure min/max functions need to support secondary extrema	The `RISE` and `FALL` features of `.MEASURE` do not work consistently for noisy waveforms. Every sign change in the waveforms slope is interpreted as the start of a new rise or fall.
469-SON: Belos memory consumption on FreeBSD and excessive CPU on other platforms	Memory or thread bloat can result when using multithreaded dense linear algebra libraries, which are employed by Belos. If this situation is observed, either build **Xyce** with a serial dense linear algebra library or use environment variables to control the number of spawned threads in a multithreaded library.
468-SON: It should be legal to have two model cards with the same model name, but different model types.	SPICE3F5 and ngspice only require that model cards of the same type have unique model names. They accept model cards of different types with the same name. **Xyce** requires that all model card names be unique.
250-SON: NODESET in **Xyce** is not equivalent to NODESET in SPICE	As currently implemented, `.NODESET` applies the initial conditions given throughout a full nonlinear solve for the operating point, then uses the result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to **Xyce**'s `.NODESET` failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround.
247-SON: Expressions don't work on .options lines	Expressions enclosed in braces ({ }) are handled specially throughout **Xyce**, and may only be used in certain contexts such as in device model or instance parameters or on `.PRINT` lines.
49-SON Xyce BSIM models recognize the model TNOM, but not the instance TNOM	

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Defect	Description
37-SON: Connectivity checking is broken for devices with more than 10 leads	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If your circuit has that type of large, highly-connected mutual inductor and the code exits with an error message, this bug may be the source of the problem. The error message now includes a recommendation to use the workaround below. ***Workaround***: Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
27-SON: Fix handling of .options parameters	When specifying .options for a particular package, what gets applied as the non-specified default options might change.
1962-SRN: Voltages from interface nodes for subcircuits may not work correctly in expressions on `.PRINT` lines	An expression that uses a voltage from an interface node to a subcircuit on a `.PRINT` line may only work if that voltage node is also used outside of the expression on the `.PRINT` line. A simple example is as follows. The expression `{V(X1:a)*I(X1:R1)}` prints out as 0, unless `V(X1:a)` is also on the `.PRINT` line.
1923-SRN: LC lines run out of memory, even if equivalent (larger) RLC lines do not.	In some cases, circuits that run fine using an RLC approximation for a transmission line, exit with an out-of-memory error if the (supposedly smaller) LC approximation is used.

1903-SRN: **Xyce** fails to collect several inductors into a linear mutual inductor	In some rare cases with complex include file usage, the mutual inductor syntax with multiple couplings can fail to work. **Xyce** will return an error message that it can not find `L_L1`:
	`L_L1 node1 node1 inductance1`
	`L_L2 node3 node4 inductance2`
	`L_L3 node5 node6 inductance3`
	`L_L4 node7 node8 inductance4`
	`K_K1 L_L1 L_L2 L_L3 L_L4 .999`

1595-SRN: **Xyce** won't allow access to inductors within subcircuits for mutual inductors external to subcircuits	It is not possible to have a mutual inductor outside of a subcircuit couple to inductors in a subcircuit. ***Workaround***: Put all inductors and mutual inductance lines that couple to them together at the same level of circuit hierarchy.

Supported Platforms

Certified Support

The following platforms have been subject to certification testing for the **Xyce** version 6.4 release.

- Red Hat Enterprise Linux® 5, x86 (serial only) and x86-64 (serial and parallel)
- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X Yosemite, x86-64 (serial and parallel)

Note that this is the last release with Certified Support for Red Hat Enterprise Linux® 5. In subsequent releases, RHEL5 will be in the "Build Support" category.

Build Support

Though not certified platforms, **Xyce** has been known to run on the following systems.

- FreeBSD 9.x and 10.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux
- Microsoft Windows under Cygwin and MinGW.

Xyce Release 6.4 Documentation

The following **Xyce** documentation is available on the **Xyce** website in pdf form.

- **Xyce** Version 6.4 Release Notes (this document)
- **Xyce** Users' Guide, Version 6.4
- **Xyce** Reference Guide, Version 6.4
- **Xyce** Mathematical Formulation
- Application Node: Using Open Source Schematic Capture Tools with **Xyce**
- Application Note: Power Grid Modeling With **Xyce**

Also included at the **Xyce** website as web pages are the following.

- Building Guide (instructions for building Xyce from the source code)
- Running the **Xyce** Regression Test Suite
- Frequently Asked Questions

External User Resources

- Website: http://xyce.sandia.gov
- Google Groups discussion forum: https://groups.google.com/forum/#!forum/xyce-users
- Email support: xyce@sandia.gov
- Address:

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