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Xyce™ Parallel Electronic Simulator Release Notes Release 6.3

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Abstract

The highlights of the ***Xyce***™ 6.3 release are documented.

Contents

Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds
- Incompatibilities With Other Circuit Simulators
- Hardware and software requirements

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at `http://xyce.sandia.gov/`.

New Features and Enhancements

Highlights for **Xyce** Release 6.3 include:

- New devices (MEXTRAM version 504, BSIM 6.1.0 and TEAM Memristor added).
- DC operating point strategy now applies source-stepping if other attempts fail.
- New devices (Branch, Bus shunt, Transformer and Generator Bus) for modeling steady-state power flow in electric power grids.
- ADMS back-end enhanced to generate code for analytic sensitivity derivatives.
- Support for measure statements when `.STEP` is used.
- The ability to re-measure existing data in `.PRN` files.
- New multi-tone Harmonic Balance (HB) analysis.
- Small signal noise analysis (`.NOISE`).

For details of each of these new features, see the **Xyce** Users' Guide, the **Xyce** Installation Guide, and the **Xyce** Reference Guide. A more complete listing of new features and improvements is given in the following sections.

Robustness Improvements

- DC operating point solution strategy now includes SPICE-like source stepping if Newton or GMIN stepping fail.
- Extensive bug fixes and usability improvements for .MEASURE. This includes user-configurable output precision, and more informative output to standard output and log files.

New Devices

- BSIM6 version 6.1.0
- MEXTRAM version 504.11.0
- TEAM Memristor
- Power Grid Branch, Bus Shunt, Transformer and Generator Bus

Interface Improvements

- Analytic derivatives are now computed for all ADMS-generated devices (VBIC, FBH HBT, MEXTRAM, BSIM6, BSIMCMG, PSP, EKV). Sensitivities computed for these devices will be more accurate than the finite-difference method used prior to this implementation.
- ADMS back-end improved to more correctly support Verilog-A ternary operators.

Defects of Release 6.2 Fixed in this Release

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
244-SON: A handful of parameter defaults in the BSIM SOI v3.2 device were incorrect	The `CGDO`, `CGSO`, `K1` and `K2` parameters had incorrect defaults. The parameter defaults have been updated to match the correct values.
277-SON: Create infrastructure for doing true SPICE-like "source stepping" in **Xyce**	When doing a DC operating point solve in SPICE, it first attempts standard Newton's method to solve the problem. If that fails, it attempts GMIN stepping, and if that fails it attempts source stepping (scaling all DC sources in the circuit iteratively from 0 to their nominal values). Until release 6.3, **Xyce** had not implemented source stepping in its own solution strategy. **Xyce** now attempts source stepping on DC solves if Newton and GMIN stepping both fail.
359-SON: scaleParam function doesn't work properly	**Xyce** 6.2 supported a "VSRCSCALE" parameter that could have been used to simulate SPICE's "source stepping" technique, but attempting to use this parameter in continuation didn't apply it properly. As of release 6.3, the VSRCSCALE continuation parameter is now properly applied to all DC sources as expected.

466-SON: .RESULT output doesn't recognize .param parameters	As an example, consider:
	`.param par1=1.0`
	`.param par2=2.0`
	`.result {par1/par2}`
	In prior releases, the code would run for a while and then when the first .RESULT output was processed (at the end of the first .STEP iteration) it would exit with an error, claiming that par1 and par2 are not recognized variables. This has been fixed in Release 6.3.

477-SON: Internal variables are not accessible inside expressions	An internal variable, accessed via n(), was not properly resolved in an expression. As an example, this failed parsing in prior releases: `.print tran {n(yneuron!neuron1_V1)}`
534-SON: .option outputs can print duplicate time points	When .options outputs were used in the netlist, the output could have had duplicate time points depending on the frequency used in the simulation and the output interval specified. Duplication of output time points no longer occurs in **Xyce** 6.3.
544-SON: Initial condition statement results in failed simulation	In versions 6.1 and older of **Xyce**, any .IC statements within a subcuit were ignored in favor of the value provided from the device line. This behavior has been restored in **Xyce** 6.3.

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
546-SON: TNOM handled incorrectly by capacitor	The capacitor in **Xyce** allows specification of the temperature-dependence of the capacitance via the `TNOM`, `TC1`, and `TC2` model parameters. In versions of **Xyce** prior to 6.3, the TNOM value was ignored and always replaced with the device package default value (27 degrees C, or the value specified in a `.OPTIONS DEVICE` line). As of **Xyce** 6.3, the capacitor no longer ignores a user-specified `TNOM` value.
550-SON: The DERIVATIVE Measure in **Xyce** is actually a Slope Measurement Between Two Endpoints	This was an incorrect definition of a derivative. As of **Xyce** 6.3, **Xyce** now supports calculating the derivative of a waveform at either a user-specified time (`AT=<time>`) or when a user-specified condition occurs (`WHEN v(1)=<value>`).
560-SON: Too many '.ENDS' does not inform used of location of problem	**Xyce** now informs the user of the file and line number where the extra .ENDS occurs.
580-SON: Supernoding capability broken in **Xyce** 6.2.	Supernoding is the ability to remove devices attached to the same node or resistors with zero resistances. This capability was disabled in **Xyce** 6.2. It has been fixed for **Xyce** 6.3, and can be used by specifying `.options topology supernode=true` in any netlist.
605-SON: MPI hang on exit on some platforms	On a handful of "build supported" platforms using OpenMPI 1.8.x, Xyce's method of exit on parsing error sometimes tripped an obscure race condition in MPI, leaving mpirun hanging even though all **Xyce** processes had exited. The method of exit in this event was changed to rely only on well-defined behaviors of MPI and this race condition is no longer tripped.
609-SON: No-op code in MOSFET6	The MOSFET6 code had an extraneous semicolon that rendered part of the `Von` expression as a no-op. This semicolon was present in the original SPICE3F5 implementation and was copied over into **Xyce** when MOS6 was implemented. ***Solution***: The extraneous semicolon was removed and the expression is no longer a no-op. This causes the "sigma" model parameter (which defaults to zero) to impact the `Von` expression as it was intended to do (and as it does in other simulators such as ngspice, where this error was corrected).

Table 1: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description

1957-SRN and 575-SON: **Xyce** not handling multiply-coupled mutual inductor correctly	`K` lines with more than two inductors were not properly creating the couplings between all inductors as stated in the reference guide.
	
	`L1 node1 node1 inductance1`
	`L2 node3 node4 inductance2`
	`L3 node5 node6 inductance3`
	`L4 node7 node8 inductance4`
	`K_K1 L1 L2 L3 L4 .999`
	
	should be equivalent to
	
	`L1 node1 node1 inductance1`
	`L2 node3 node4 inductance2`
	`L3 node5 node6 inductance3`
	`L4 node7 node8 inductance4`
	`K_K12 L1 L2 .999`
	`K_K13 L1 L3 .999`
	`K_K14 L1 L4 .999`
	`K_K23 L2 L3 .999`
	`K_K24 L2 L4 .999`
	`K_K34 L3 L4 .999`
	
	In all versions of **Xyce** prior to 6.3, only the snippet with multiple `K` lines produced the correct results. The other version improperly coupled only coupled L1 to L2 and L3 to L4.

1945-SRN: Ending subcircuit with .END, not .ENDS, results in an application hang	An error message now indicates the location of the .END statement.

Known Defects and Workarounds

Table 2: Known Defects and Workarounds.

Defect	Description
27-SON: Fix handling of .options parameters	When specifying .options for a particular package, what gets applied as the non-specified default options might change.
37-SON: Connectivity checking is broken for devices with more than 10 leads	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If your circuit has that type of large, highly-connected mutual inductor and the code exits with an error message, this bug may be the source of the problem. The error message now includes a recommendation to use the workaround below. ***Workaround***: Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
49-SON Xyce BSIM models recognize the model TNOM, but not the instance TNOM	
247-SON: Expressions don't work on .options lines	Expressions enclosed in braces ({ }) are handled specially throughout **Xyce**, and may only be used in certain contexts such as in device model or instance parameters or on `.PRINT` lines.
250-SON: NODESET in **Xyce** is not equivalent to NODESET in SPICE	As currently implemented, .NODESET applies the initial conditions given throughout a full nonlinear solve for the operating point. It then uses that result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to Xyce's .NODESET failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround.

Table 2: Known Defects and Workarounds.

Defect	Description
468-SON: It should be legal to have two model cards with the same model name, but different model types.	SPICE3F5 and ngspice only require that model cards of the same type have unique model names. They accept model cards of different types with the same name. **Xyce** requires that all model card names be unique.
469-SON: Belos memory consumption on FreeBSD and excessive CPU on other platforms	Memory or thread bloat can result when using multithreaded dense linear algebra libraries, which are employed by Belos. If this situation is observed, either build **Xyce** with a serial dense linear algebra library or use environment variables to control the number of spawned threads in a multithreaded library.
583-SON: Switch with RON=0 leads to convergence failure.	The switch device does not prevent a user from specifying `RON=0` in its model, but then takes the inverse of this value to get the "on" conductance. The resulting invalid division will either lead to a division by zero error on platforms that throw such errors, or produce a conductance with "Not A Number" or "Infinity" as value. This will lead to a convergence failure. ***Workaround***: Do not specify an identically zero resistance for the switch's "on" value. A small value of resistance such as 1e-15 or smaller will generally work well as a substitute.
620-SON: TO, FROM and TD Qualifiers Function Incorrectly in the FREQ Measure	The use of these qualifiers in a `FREQ` measure statement may give an incorrect measurement window. This is noted in the Reference Guide.
621-SON: FIND-WHEN Measure in **Xyce** Only Correctly Supports the WHEN Syntax. FIND-WHEN is incorrect.	An example is given in the HSpice Compatibility subsection of the `.MEASURE` section of the Reference Guide.
1595-SRN: **Xyce** won't allow access to inductors within subcircuits for mutual inductors external to subcircuits	It is not possible to have a mutual inductor outside of a subcircuit couple to inductors in a subcircuit. ***Workaround***: Put all inductors and mutual inductance lines that couple to them together at the same level of circuit hierarchy.

1903-SRN: **Xyce** fails to collect several inductors into a linear mutual inductor	In some rare cases with complex include file usage, the mutual inductor syntax with multiple couplings can fail to work. **Xyce** will return an error message that it can not find `L_L1` in this example:
	`L_L1 node1 node1 inductance1`
	`L_L2 node3 node4 inductance2`
	`L_L3 node5 node6 inductance3`
	`L_L4 node7 node8 inductance4`
	`K_K1 L_L1 L_L2 L_L3 L_L4 .999`

1923-SRN: LC lines run out of memory, even if equivalent (larger) RLC lines do not.	In some cases, circuits that run fine using an RLC approximation for a transmission line, exit with an out-of-memory error if the (supposedly smaller) LC approximation is used.

Resolved Incompatibilities With Other Circuit Simulators

Table 3 lists incompatibilities between Xyce and other circuit simulators that were resolved in this release. Please consult the Xyce Reference Guide for a list of known incompatibilities, and how to work around them.

Table 3: Resolved incompatibilities with other circuit simulators.

Issue	Comment
Some parameter defaults in the BSIM SOI v3.2 device did not match SPICE.	The `CGDO`, `CGSO`, `K1` and `K2` parameters now have the correct defaults.

Important Changes to **Xyce** Usage Since the Release 6.2.

Table 4 lists some usage changes for **Xyce**.

Table 4: Changes to netlist specification since the last release.

Issue	Comment
Change in `NUMFREQ` usage in .options hbint for Harmonic Balance analysis	`NUMFREQ` is no longer required to be an odd number. It now specifies the number of positive harmonics for each tone.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 6.3.

Supported Platforms (Certified Support)

Xyce 6.3 currently supports any of the following operating system platforms (all versions imply the earliest supported—**Xyce** generally works on later versions as well). These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 6.3 release.

- Red Hat Enterprise Linux® 5, x86 (serial only) and x86-64 (serial and parallel)
- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X, x86-64 (serial and parallel)
- TLCC (serial and parallel)
- Red Sky (serial and parallel)

Build Supported Platforms (not Certified)

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 6.3 release. Despite this lack of testing rigor, **Xyce** has been known to run under these configurations.

- FreeBSD 9.x and 10.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux
- Microsoft Windows under Cygwin and MinGW.

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The **Xyce** team has not determined a minimum memory or processor speed requirement. Any modern computer should have enough memory and processor power to run moderately sized circuits in serial with **Xyce**. Naturally, memory requirements grow with problem size.

Running **Xyce** in parallel will require a system with at least two processors. For problems of the size where parallel operation is beneficial (thousands of devices per processor), one can expect to need several gigabytes of memory per processor.

For the very largest problems that **Xyce** can run (millions of devices), one will require a cluster system with a sufficient number of nodes to distribute the problem efficiently, and sufficient memory per node to support the distributed problem.

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the **Xyce** binary have no run-time software requirements, as they ship with all the shared libraries they need. However, parallel versions require Open MPI (http://www.open-mpi.org/) (version 1.4 or higher) at run time. TLCC and Red Sky users can load the **xyce** module to properly set the environment.

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. A complete list of these required libraries is available in the building guide on the **Xyce** web site.

Xyce Release 6.3 Documentation

The following **Xyce** documentation is available at the **Xyce** website in pdf form.

- **Xyce** Release Notes, Version 6.3 (this document)
- **Xyce** Users' Guide, Version 6.3
- **Xyce** Reference Guide, Version 6.3
- **Xyce** Mathematical Formulation
- Application Node: Using Open Source Schematic Capture Tools with **Xyce**

Also included at the **Xyce** website as web pages are the following.

- Building Guide (instructions for building Xyce from the source code)
- Running the Xyce Regression Test Suite
- Frequently Asked Questions

Device Support

Table 5 contains a complete list of devices for **Xyce** Release 6.3.

Table 5: Devices Supported by Xyce

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Stability improvements to Sandia Core model (not fully PSpice compatible)
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSpice enhancements

Table 5: Devices Supported by Xyce

Device	Comments
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model, version 1.2
Bipolar Junction Transistor (BJT) (Level 23)	FBH (Ferdinand-Braun-Institut für Höchstfrequenztechnik) HBT model, version 2.1
Bipolar Junction Transistor (BJT) (Level 504)	MEXTRAM version 504.11 **New!**
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	SPICE level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	SPICE level 6 MOSFET
MOSFET (Level 9)	BSIM3 model
MOSFET (Level 10)	BSIM SOI model
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 77)	BSIM6 model version 6.1.0 **New!**
MOSFET (Level 103)	PSP model
MOSFET (Level 107)	BSIM-CMG version 107.0.0
MOSFET (Level 301)	EKV model version 3.0.1
Transmission Line (TRA)	Lossless
Transmission Line (LTRA)	Lossy
Lumped Transmission Line	Lossy or Lossless

Table 5: Devices Supported by Xyce

Device	Comments
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
Power Grid	Separate models for Branch, Bus Shunt, Transformer and Generator Bus **New!**
Memristor	TEAM formulation **New!**

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Xyce's expression library is based on that inside Spice 3F5 developed by the EECS Department at the University of California.

The EKV3 MOSFET model was developed by the EKV Team of the Electronics Laboratory-TUC of the Technical University of Crete.

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