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Xyce™ Parallel Electronic Simulator Release Notes Release 6.2

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Abstract

The highlights of the ***Xyce***™ 6.2 release are documented.

Contents

Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds
- Incompatibilities With Other Circuit Simulators

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://xyce.sandia.gov/.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 6.2.

Supported Platforms (Certified Support)

Xyce 6.2 currently supports any of the following operating system platforms (all versions imply the earliest supported—**Xyce** generally works on later versions as well). These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 6.2 release.

- Red Hat Enterprise Linux® 5, x86 (serial only) and x86-64 (serial and parallel)
- Red Hat Enterprise Linux® 6, x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X, x86-64 (serial and parallel)
- TLCC (serial and parallel)
- Red Sky (serial and parallel)

Build Supported Platforms (not Certified)

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 6.2 release. Despite this lack of testing rigor, **Xyce** has been known to run under these configurations.

- FreeBSD 9.x on Intel x86 and x86-64 architectures (serial and parallel)
- Distributions of Linux other than Red Hat Enterprise Linux
- Microsoft Windows under Cygwin and MinGW.

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The **Xyce** team has not determined a minimum memory or processor speed requirement. Any modern computer should have enough memory and processor power to run moderately sized circuits in serial with **Xyce**. Naturally, memory requirements grow with problem size.

Running **Xyce** in parallel will require a system with at least two processors. For problems of the size where parallel operation is beneficial (thousands of devices per processor), one can expect to need several gigabytes of memory per processor.

For the very largest problems that **Xyce** can run (millions of devices), one will require a cluster system with a sufficient number of nodes to distribute the problem efficiently, and sufficient memory per node to support the distributed problem.

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the **Xyce** binary have no run-time software requirements, as they ship with all the shared libraries they need. However, parallel versions require Open MPI (`http://www.open-mpi.org/`) (version 1.4 or higher) at run time. TLCC and Red Sky users can load the **xyce** module to properly set the environment.

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 11.10.2 (`http://trilinos.org`). Trilinos is a suite of packages that includes solver and partitioning libraries in parallel and serial, in addition to many other utilites.

- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (http://www.cise.ufl.edu/research/sparse/umfpack/). This is also provided by the SuiteSparse package that is available on many systems.

- BLAS (Basic Linear Algebra Subprograms). This may be included with the compiler, or it may require separate package installation. One may also use ATLAS (http://math-atlas.sourceforge.net).

- LAPACK (Linear Algebra PACKage). This may be included with the compiler, or it may require separate package installation. One may also use ATLAS (http://math-atlas.sourceforge.net).

For parallel builds, the following libraries are additionally required:

- Open MPI (http://www.open-mpi.org) library for message passing (version 1.4 or higher). The version used to build Xyce must be the same that is used for building Trilinos.

- ParMETIS (http://glaros.dtc.umn.edu/gkhome/metis/parmetis/overview) library for graph partitioning (version 3.1 or higher). The MPI compiler used to compile ParMETIS must be the same that is used for Trilinos and Xyce.

Xyce Release 6.2 Documentation

The following **Xyce** documentation is available at the **Xyce** website in pdf form.

- **Xyce** Release Notes, Version 6.2 (this document)

- **Xyce** Users' Guide, Version 6.2

- **Xyce** Reference Guide, Version 6.2

- **Xyce** Mathematical Formulation

- Application Node: Using Open Source Schematic Capture Tools with **Xyce**

Also included at the **Xyce** website as web pages are the following.

- Building Guide (instructions for building Xyce from the source code)

- Running the Xyce Regression Test Suite

- Frequently Asked Questions

New Features and Enhancements

Highlights for **Xyce** Release 6.2 include:

- Transient direct sensitivities.
- Support lead current calculation and output for Harmonic Balance (HB) analysis.
- Improved interpolation for both the Trapezoid and Gear time integrators.
- Improved results output (.PRINT) capabilities.
- Lumped tranmission line model.
- Support for a new digital latch (DLTCH) model.
- Multiple .PRINT's result in multiple output files.
- GMIN stepping is attempted automatically if the initial attempt to find a DC operating point fails.
- "%" no longer a reserved character in names.
- "!" is a reserved character in names to separate device name from ancillary information.

For details of each of these new features, see the **Xyce** Users' Guide, the **Xyce** Installation Guide, and the **Xyce** Reference Guide. A more complete listing of new features and improvements is given in the following sections.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 6.2.

Table 1: Devices Supported by Xyce

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Stability improvements to Sandia Core model (not fully PSpice compatible)
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSpice enhancements
Independent Voltage Source (VSRC)	

Table 1: Devices Supported by Xyce

Device	Comments
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model, version 1.2
Bipolar Junction Transistor (BJT) (Level 23)	FBH (Ferdinand-Braun-Institut für Höchstfrequenztechnik) HBT model, version 2.1
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	SPICE level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	SPICE level 6 MOSFET
MOSFET (Level 9)	BSIM3 model
MOSFET (Level 10)	BSIM SOI model
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 103)	PSP model
MOSFET (Level 107)	BSIM-CMG version 107.0.0
MOSFET (Level 301)	EKV model version 3.0.1
Transmission Line (TRA)	Lossless
Transmission Line (LTRA)	Lossy
Lumped Transmission Line	Lossy or Lossless **New!**
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled

Table 1: Devices Supported by Xyce

Device	Comments
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines

New Devices

- Digital latch model (DLTCH).
- Lumped transmission line model.

Enhanced Solver Stability, Performance and Features

- Transient direct sensitivity analysis. This is an enhancement to `.SENS`, which previously only applied to steady-state (.DC) analysis.
- New nonlinear solution strategy similar to SPICE, so that when the standard Newton method fails to get a DC Operating Point (DCOP), GMIN stepping is automatically attempted. This new strategy is now default behavior in **Xyce**.

Defects of Release 6.1 Fixed in this Release

Table 2: Fixed Defects. Note that we have two different Bugzilla systems for Sandia users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
351-SON: .MEASURE console output by every processor in parallel.	When .MEASURE is used in parallel, every processor outputs to the console. However only the root processor's output might appear in the "***Measure functions***" part of the output file. The rest of the .MEASURE output could be scattered around and mixed with the execution statistics. ***Solution***: Only the root processor outputs the .MEASURE results.
368-SON: Fix and document the REPEAT feature of the PWL transient specification	The repeat (`R`) and time delay (`TD`) features of the Piecewise Linear voltage or current source, PWL, were undocumented and did not work correctly. ***Solution***: This is fixed but partially incompatible with HSpice syntax since `R` (without the `=0`), to mean repeat the waveform starting at time=0, is legal in HSpice. **Xyce** requires `R=0`, in that case. The **Xyce** syntax for PWL sources is not compatible with PSpice's REPEAT syntax.
380-SON: Measure statements need to support expressions	The variable that .measure used in a calculation had to be a solution or state/store variable. Expressions, such as `max(v(node1)-v(node2))` were not allowed. ***Solution***: This is fixed.
384-SON: Errors compiling **Xyce** with Bison 3.0.	Bison 3.0 deprecated access to identifiers that **Xyce** used for error reporting. ***Solution***: This is fixed and **Xyce** should compile with either Bison 2.7 or Bison 3.0.x.
427-SON: Certain subcircuit nodes cannot be accessed in expressions	**Xyce** allows nodes within a subcircuit to be referenced in expressions and on .print lines using the syntax "<subcircuit instance name>:<nodename>". This works on .print lines even if the node named is one that is on the subcircuit declaration line (i.e., dummy argument nodes, which are just aliases for names in the calling circuit context). This does not work inside expressions. ***Solution***: These values are now accessible within expressions.
438-SON: .step output for HB in Standard (.prn) format does not reset Index for each step or otherwise mark new step data	It is difficult to separate the results, in an .HB.FD.prn file, for each step because the Index column is monotonic instead of resetting to zero at the beginning of each step, as in transient or DC analysis runs. ***Solution***: The index is now reset at the start of each .STEP.
439-SON: Interpolation does not work well with TRAP and GEAR	The problem occurs in certain situations when the output is interpolated. For Trap, the problem can occur when the 2nd order Trap is used. For Gear, the problem occurs when the lead currents are interpolated. ***Solution***: This is fixed.

Table 2: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
441-SON: `.AC` output for step-tecplot is wrong.	When using STD output, **Xyce** would create both `netlist.cir.FD.prn` and `netlist.cir.prn` files. When using tecplot output, **Xyce** would only create one file, `netlist.cir.dat`. ***Solution***: This is fixed.
442-SON: lead currents are not correctly output for HB analysis	The lead currents were not calculated in HB analysis. The output would be all zeros for the lead currents in HB analysis. ***Solution***: This is fixed.
483-SON: ASCII rawfile output does not work with .dc without the -r flag.	Running `Xyce -a <filename>` resulted in a file in binary format, rather than ASCII. However, using both the `-r <rawfile>` and `-a` flags resulted in the `<rawfile>` being in ASCII format. ***Solution***: This is fixed.
484-SON: Putting resistor parameter on `.PRINT` line, with homotopy simulation causes segfault	Including `RC:R` on the `.PRINT` line caused **Xyce** to seg-fault. ***Solution***: This is fixed.
487-SON: `.OP` with PDE devices gives a seg fault	In some circuits with PDE devices, `.OP` would cause **Xyce** to crash. ***Solution***: This is fixed.
488-SON: HB-specific output should be excluded from the *.hb_ic.prn file	If the following HB print line `.print HB VDB(1)` was used then the output files associated with the initial condition (which are the transient output files) would print `-inf` for VDB. This caused problems with Tecplot. ***Solution***: This can be resolved by by adding an `HB_IC` output specifier. Please see the **Xyce** Reference Guide, Version 6.2 for more details.
493-SON: Ill-formed Source Definitions Cause a Core Dump	A source definition without any parameters caused a core dump. An example instance line was: `V1 1 0 sin` ***Solution***: This is fixed.
494-SON: Remove metacharacters (%) in the specification of devices and variables	**Xyce** used % as a white space filler for various internal variables. So, the use of % in device names (which is legal in other SPICE-like circuit simulators) would have unpredictable results in **Xyce**. ***Solution***: % is now a legal character in a **Xyce** device names.
496-SON: Calling RAND() from within a user defined function causes a segmentation fault	An external user reported that using `RAND()` in a user defined function caused **Xyce** to crash with a segmentation fault. ***Solution***: This is fixed.

Table 2: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
497-SON: FILE keyword in voltage/current source PWL function doesn't work in lower case.	The Piecewise Linear function for a voltage or current source, PWL, can read its data from a file with the syntax: `ImySource 1 0 PWL FILE "mydata.dat"`. If the FILE keyword was in lower case text as in "file" then **Xyce** emitted an error. ***Solution***: This is fixed in the parser.
507-SON: Parser bottleneck for .PRINT lines with many arguments	An external user wanted to output the lead current through every resistor in a very large (more than 1M device) circuit. This caused **Xyce** to get stuck during the .PRINT line processing. ***Solution***: This is fixed in the parser.
511-SON: Remove Unused .OUTPUT feature.	.output was obsolete code that was not documented in the **Xyce** User Guide or Reference Guide. It was the predecessor of the currently documented mechanism for specifying output intervals, .options output. ***Solution***: This was feature was removed from the parser. Consult the **Xyce** Reference Guide, Version 6.2 for the syntax for .options output instead.
518-SON: Non-Linear Mutual Inductor should cleanly handle magnetic moment equation	The non-linear mutual inductor adds an equation for the magnetic moment of the device to the system of equations. If the user specifies model parameters where the gap is zero and the domain flexing parameter is small, (e.g., `C` $\ll$ `0.1`), then the magnetic moment equation becomes very similar to the sum of the current derivatives equation (R(t) in **Xyce**'s formulation). This can cause the simulation to be unstable. ***Solution***: The non-linear mutual inductor drops the magnetic moment equation from the system of equations it adds when the domain flexing parameter (`C`) is below a user settable limit (`CLIM`). The user can recover **Xyce**'s previous behavior by setting `CLIM` to zero. The defaults are `CLIM=0.005` and `C=0.2`.
519-SON: Raw file outputs zero for resistor lead current	An open source customer reported that **Xyce** was improperly outputting lead currents in the rawfile format. When run with "Xyce -a netlist", the ascii rawfile always showed I(R1)= zero. Replacing the .print line with a default format (removing FORMAT=RAW and FILE=foobar.raw) produced a standard columnar output file with the correct lead current in it. ***Solution***: This is fixed.
1788-SRN: Make level 57 synonym for level 10 mosfet	This is a compatibility request to better accomodate SmartSpice and HSpice users. ***Solution***: **Xyce** provide partial compatibility that is adequate for internal Sandia users. In most SPICE-like codes, `level=57` is the BSIM4 SOI. In **Xyce**, `level=57` is the BSIM3 SOI.

Table 2: Fixed Defects. Note that we have two different Bugzilla systems for Sandia Users. SON, which is on the open network, and SRN, which is on the restricted network.

Defect	Description
1922-SRN: **Xyce** nonlinear core model defaults seriously underestimate hysteresis effects for small signals	The magnetic core model has some parameter defaults that effectively turn off magnetic effects when small-amplitude driving signals are applied. ***Solution***: The performance of the **Xyce** non-linear mutual inductor model has been improved for small-signal inputs. Please consult the Inductor section of the **Xyce** Reference Guide for more details on the usage of the `DEVSCALING` and `CONSTANTDEVSCALING` parameters.

Known Defects and Workarounds

Table 3: Known Defects and Workarounds.

Defect	Description
27-SON: Fix handling of .options parameters	When specifying .options for a particular package, what gets applied as the non-specified default options might change.
37-SON: Connectivity checking is broken for devices with more than 10 leads	The diagnostic code used by the **Xyce** setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If your circuit has that type of large, highly-connected mutual inductor and the code exits with an error message, this bug may be the source of the problem. The error message now includes a recommendation to use the workaround below. ***Workaround***: Disable connectivity checking by adding the line `.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0` to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.
49-SON Xyce BSIM models recognize the model TNOM, but not the instance TNOM	
195-SON: Restart files are not produced if initial_interval is not specified	The users' guide states that if `.OPTIONS RESTART` is specified without an `INITIAL_INTERVAL` that the restart file will be saved at every time step. This is not working, and if no initial interval is specified, no restart is saved at all. ***Workaround***: Always specify a suitable initial interval when requesting restart.
244-SON: The defaults in Xyce bsimsoi do not match defaults in spice3 bsimsoi	Some of the default parameters used in the BSIM3 SOI (level 10) MOSFET do not match SPICE3F5's defaults, leading to observed differences in behavior if a model card does not specify these parameters. ***Workaround***: The parameters at issue appear all to be parameters that have *computed* rather than hard-coded defaults. These include `CGDO`, `CGSO`, `K1`, `K2`, `XJ`. It is best to use extracted values for these parameters rather than relying on the defaults until this bug is fixed.

Table 3: Known Defects and Workarounds.

Defect	Description
247-SON: Expressions don't work on .options lines	Expressions enclosed in braces ({ }) are handled specially throughout Xyce, and may only be used in certain contexts such as in device model or instance parameters or on `.PRINT` lines.
250-SON: NODESET in xyce is not equivalent to NODESET in SPICE	As currently implemented, .NODESET applies the initial conditions given throughout a full nonlinear solve for the operating point, then uses the result as an initial guess for a second nonlinear solve with no constraints. This is not the same as SPICE, which merely applies the given initial conditions to a single nonlinear solve for the first two iterations, then lets the problem converge with no further constraints. This can lead to Xyce's .NODESET failing where the same netlist in SPICE might not, if the initial conditions are such that a full nonlinear solve cannot converge with those constraints in place. There is no workaround.
365-SON: Missing Default Instance Length Parameter in Resistor Model Parameters	The resistor allows a semiconductor resistor formulation given a sheet resistance, length, and width, but no reasonable default is given for the length. A default width parameter is provided through the model card, and is used if no width is specified on the instance line. ***Workaround***: Always specify a length on the instance line for any resistor for which the semiconductor resistor syntax is used (see the **Xyce** Reference Guide for usage).

466-SON: .RESULT output doesn't recognize .param parameters	As an example, consider:
	
	`.param par1=1.0`
	`.param par2=2.0`
	`.result {par1/par2}`
	
	The code will run for a while, and then when the first .RESULT output is processed (at the end of the first .STEP iteration) it will exit with an error, claiming that par1 and par2 are not recognized variables.
	This .print line does work though:
	
	`.print tran {par1/par2}`

468-SON: It should be legal to have two model cards with the same model name, but different model types.	SPICE3F5 and ngspice only require that model cards of the same type have unique model names. They accept model cards of different types with the same name. Xyce requires that all model card names be unique.
469-SON: Belos memory consumption on FreeBSD and excessive CPU on other platforms	Memory or thread bloat can result when using multithreaded dense linear algebra libraries, which are employed by Belos. If this situation is observed, either build Xyce with a serial dense linear algebra library or use environment variables to control the number of spawned threads in a multithreaded library.

Table 3: Known Defects and Workarounds.

Defect	Description
477-SON: Internal variables are not accessible inside expressions	An internal variable, accessed via n(), is not properly resolved in an expression. As an example, this fails parsing. `.print tran {n(yneuron!neuron1_V1)}` ***Workaround***: If the braces are removed then the netlist runs without problems.
478-SON: Measure min/max functions need to support secondary extrema	The `RISE` and `FALL` features of `.MEASURE` do not work consistently for noisy waveforms. Every sign change in the waveforms slope is interpreted as the start of a new rise or fall.
1595-SRN: Xyce won't allow access to inductors within subcircuits for mutual inductors external to subcircuits	It is not possible to have a mutual inductor outside of a subcircuit couple to inductors in a subcircuit. ***Workaround***: Put all inductors and mutual inductance lines that couple to them together at the same level of circuit hierarchy.

1903-SRN: Xyce fails to collect several inductors into a linear mutual inductor	This syntax does not work. **Xyce** will return an error message that it can not find `L_L1`:
	`L_L1 node1 node1 inductance1`
	`L_L2 node3 node4 inductance2`
	`L_L3 node5 node6 inductance3`
	`L_L4 node7 node8 inductance4`
	`K_K1 L_L1 L_L2 L_L3 L_L4 .999`

1923-SRN: LC lines run out of memory, even if equivalent (larger) RLC lines do not.	In some cases, circuits that run fine using an RLC approximation for a transmission line, exit with an out-of-memory error if the (supposedly smaller) LC approximation is used.

Resolved Incompatibilities With Other Circuit Simulators

Table 4 lists incompatibilities between Xyce and other circuit simulators that were resolved in this release. Please consult the Xyce Reference Guide for a list of known incompatibilities, and how to work around them.

Table 4: Resolved incompatibilities with other circuit simulators.

Issue	Comment
PSpice models cards for resistors, capacitors and inductors.	`R` and `RES` are now synonyms in `.MODEL` statements for resistors. `C` and `CAP` are now synonyms in `.MODEL` statements for capacitors. `L` and `IND` are now synonyms in `.MODEL` statements for inductors.

Important Changes to **Xyce** Usage Since the Release 6.1.

Table 5 lists some usage changes for **Xyce**.

Table 5: Changes to netlist specification since the last release.

Issue	Comment
Multiple .PRINT's allowed	Mutiple .PRINT's are now allowed in the netlist. .PRINT commands appropriate for the current analysis are enabled and may result in multiple output files being concurrently generated, each with a different variable list and format.
Change in reserved characters in names	"%" is no longer a reserved character in names. "!" is now a reserved character in names.

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Xyce's expression library is based on that inside Spice 3F5 developed by the EECS Department at the University of California.

The EKV3 MOSFET model was developed by the EKV Team of the Electronics Laboratory-TUC of the Technical University of Crete.

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