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# **Xyce™ Parallel Electronic Simulator Release Notes**

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**Release 5.2**

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## **Xyce™ Parallel Electronic Simulator Release Notes**

### **Release 5.2**

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## Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at <http://xyce.sandia.gov/>.

## Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce 5.2**.

### Supported Platforms (Certified Support)

**Xyce 5.2** currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 5.2 release.

- Red Hat Enterprise Linux® 5, x86 and x86-64 (serial and parallel)
- Microsoft Windows 7®, x86 (serial)
- Apple® OS X, x86-64 (serial and parallel)
- TLCC (serial and parallel)
- Red Sky (serial and parallel)

### Build Supported Platforms (not Certified)

The platforms listed in this section are “not supported” in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 5.2 release.

- Xyce directly coupled to the Dakota optimization and uncertainty quantification library for Apple OS X and Linux platforms.
- FreeBSD 7.x on Intel x86 architectures (serial and parallel)

Please contact the Xyce development team for platform and configuration availability.

## Hardware Requirements

The following are *estimated* hardware requirements for running **Xyce**:

- 128MB memory minimum – *memory requirements increase with circuit size*
- 128MB disk space required for installation (does not include space needed for output files)

## Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the static **Xyce** binary have no run-time software requirements. However, parallel versions require the following software at run time:

- Open MPI (<http://www.open-mpi.org/>) (version 1.4 or higher)
- Intel (<http://www.intel.com/>) MKL (version 10.2) and Compilers (version 11.1)
- TLCC and Red Sky users can load the **xyce** module to properly set the environment

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 10.2 (Sandia, <http://trilinos.sandia.gov>) . This is a suite of libraries including Amesos, AztecOO, Belos, Teuchos, Epetra, EpetraExt, Ifpack, NOX, LOCA, Sacado, Zoltan.
- SuperLU (libsuperlu.a) (<http://crd.lbl.gov/xiaoye/SuperLU/> )
- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (<http://www.cise.ufl.edu/research/sparse/umfpack/>)
- LAPACK
- BLAS

For parallel builds, the following libraries are additionally required:

- MPI (<http://www.open-mpi.org>) library for message passing (version 1.4 or higher). The version used to build Xyce must be the same that is used for building Trilinos.
- ParMETIS (<http://glaros.dtc.umn.edu/gkhome/views/metis>) library for graph partitioning (version 3.1 or higher). The MPI compiler used to compile ParMETIS must be the same that is used for Trilinos and Xyce.

## Xyce Release 5.2 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form.

- **Xyce** Users' Guide, Version 5.2
- **Xyce** Reference Guide, Version 5.2

- **Xyce** Release Notes, Version 5.2
- **Xyce** Theory Document
- EKV MOSFET version 3.0.1 model documentation.
- **Xyce** Test Plan

## New Features and Enhancements

Highlights for **Xyce** Release 5.2 include:

- New support for PSP and EKV MOSFET models.
- Added support for PNP transistors in VBIC HBT model.
- New compact neutron model, which uses a numerical, instead of analytic, carrier model.
- New variable-order trapezoid (Adams method) algorithm.

For details of each of these new features, see the **Xyce** Users' Guide, and the **Xyce** Reference Guide. Also, a more complete listing of new features and improvements are given in the following sections.

### Device Support

Table 1 contains a complete list of devices for **Xyce** Release 5.2.

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSPICE enhancements
Diode (Level 3)	Prompt and delayed photocurrent radiation model
Diode (Level 4)	Generic photocurrent source model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	

Device	Comments
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2)	Prompt photocurrent radiation model
Bipolar Junction Transistor (BJT) (Level 3)	Neutron-effects model
Bipolar Junction Transistor (BJT) (Level 4)	Prompt photocurrent radiation model (same as level 2)
Bipolar Junction Transistor (BJT) (Level 5)	Deveney-Wrobel Neutron model, with photocurrent
Bipolar Junction Transistor (BJT) (Level 6)	Physics-based (QASPR) Neutron model, with photocurrent
Bipolar Junction Transistor (BJT) (Level 10)	Vertical Bipolar Intercompany (VBIC) model <b>Updated!</b>
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	Spice level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	Spice level 6 MOSFET
MOSFET (Level 9)	BSIM3 model with initial condition support
MOSFET (Level 10)	BSIM SOI model with initial condition support
MOSFET (Level 11)	BSIM SOI model with Transient Photocurrent
MOSFET (Level 12)	BSIM SOI model with Transient Photocurrent
MOSFET (Level 14)	BSIM4 model

Device	Comments
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 19)	VDMOS total dose radiation model
MOSFET (Level 20)	VDMOS photocurrent model
MOSFET (Level 21)	Level 1 with photocurrent
MOSFET (Level 23)	Level 3 with photocurrent
MOSFET (Level 103 )	PSP model <b>New!</b>
MOSFET (Level 301)	EKV model <b>New!</b>
Transmission Line	Lossless
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
PDE Devices (Level 3)	one-dimensional, with neutron damage physics <b>New!</b>
Digital (Level 1)	Behavioral Digital
EXT (Level 1)	External device, used for code coupling and power-node parasitics simulations
OP AMP (Level 1)	Ideal operational amplifier
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
NEUTRON (Level 1)	Stand-alone neutron device model
ROM (Level 1)	Reduced-order model device for linear (RLC) circuits

Table 1: Devices Supported by Xyce

## New Devices

- New compact neutron model, which uses a numerical, instead of analytic, carrier model. This is the level=3 pde model.
- PSP MOSFET model. This is an advanced surface-potential-based compact model for MOSFETs, developed at Pennsylvania State University and Philips Research Laboratory.
- EKV MOSFET model. This model is a scalable and compact MOSFET model developed for use in the simulation of circuits using submicron CMOS technologies.
- PNP VBIC model. The industry-standard VBIC model for Heterojunction Bipolar Transistors (HBTs) has been extended in this version of **Xyce** to support PNP devices as well as NPN.

## Defects of Release 5.1 Fixed in this Release

Defect	Description
<b>bug 1755</b> : Improve memory scalability on large circuits in parallel.	In prior releases, the input parser could exhaust memory system memory leading to a crash or stall. This was due in part to inefficient memory allocation. Memory scalability of the input parser has been greatly improved in <b>Xyce</b> version 5.2.
<b>bug 1792</b> : Broken temperature-dependent breakdown model in Level 2 diode	The PSpice-compatible diode (level 2) was not correctly computing temperature-dependent breakdown when the parameters TBV1 and TBV2 were specified. This has been fixed in <b>Xyce</b> version 5.2.
<b>bug 1801</b> : Broken handling of subcircuit parameters when passing global parameters	A bug in the input parser led to incorrect circuit behavior when a global parameter (i.e. a parameter defined in a <code>.global_param</code> statement) was passed to a subcircuit in a subcircuit parameter (e.g. one declared following a <code>PARAMETERS:</code> keyword). This bug has been fixed in <b>Xyce</b> version 5.2.
<b>bug 1806</b> : Error expanding expression in subcircuit	A bug in the input parser present in all prior versions of <b>Xyce</b> led to incorrect expansion of expressions within subcircuits that contained both subcircuit parameters and subcircuit dummy nodes, if any of the dummy nodes were connected to ground in the subcircuit instantiation. This bug has been fixed in <b>Xyce</b> version 5.2.
<b>bug 201</b> : IC= for the inductor device is busted	Previously, when IC= was applied to inductor devices, it had no effect. As of <b>Xyce</b> version 5.2, IC= will correctly apply an initial current condition on inductors.
<b>bug 1761</b> : Fix neutron device to work in parallel	Previously, the QASPR neutron model did not correctly parse its inputs in parallel simulations, and thus could only be used in serial builds of <b>Xyce</b> . As of <b>Xyce</b> version 5.2, this has been fixed.
<b>bug 1795</b> : IC= for the capacitor with NOOP causes segfault	This has been fixed. IC= on a capacitor will not cause <b>Xyce</b> version 5.2 to segfault.

Table 2: Fixed Defects.

## Known Defects and Workarounds

Defect	Description
<p>Connectivity checking is broken for devices with more than 10 leads [SON Bug 37]</p>	<p>The diagnostic code used by the <b>Xyce</b> setup that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, "Internal: lead index not found" after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If you see the error message "Internal: lead index not found." and you have such a large mutual inductor, this bug is the source of the problem.</p> <p><i>Workaround:</i> Disable connectivity checking by adding the line</p> <pre style="text-align: center;">.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0</pre> <p>to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.</p>
<p>.DC sweep output.</p>	<p>.DC sweep calculation does not automatically output sweep results.</p> <p><i>Workaround:</i> Use .PRINT statement to output sweep variable results.</p>
<p>BJT Current Crowding</p>	<p>"Timestep too small" failures can result when IRB nonzero with level 2 and level 4 BJT</p> <p><i>Workaround:</i> If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the <b>Xyce</b> development team so that this bug can be characterized and eliminated.</p>
<p>Microsoft Windows installation restrictions</p>	<p>Users with insufficient privileges (i.e. Limited Account) are not permitted to install <b>Xyce</b> into folders on the System Drive (usually C:).</p> <p><i>Workaround:</i> First, manually create the desired folder on the System Drive. It is then possible to install <b>Xyce</b> into this folder by following the standard Setup procedure.</p>

Defect	Description
Incompatible proprietary file formats.	<p>Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in <b>Xyce</b>. <b>Xyce</b> does not recognize proprietary file formats. <i>Workaround:</i> It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.</p>
One known instance of restart results not matching original run results.	<p>There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range.  <i>Workaround:</i> The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.</p>
Infinite-slope transitions in B-sources causes "time step too small" errors [bug 772]	<p>The nonlinear dependent source ("B-source") allows the user to specify expressions that could have infinite-slope transitions, such as</p> <pre>Bcrt1 OUTA 0 V={ IF( (V(IN) &gt; 3.5), 5, 0 ) }</pre> <p>This can lead to "timestep too small" errors when <b>Xyce</b> reaches the transition point. Infinite-slope transitions in expressions dependent only on the <code>time</code> variable are a special case, because <b>Xyce</b> can detect that they are going to happen in the future and set a "breakpoint" to capture them. Infinite-slope transitions depending on other solution variables cannot be predicted in advance, and cause the time integrator to scale back the timestep repeatedly in an attempt to capture the feature until the timestep is too small to continue.  <i>Workaround:</i> Do not use step-function or other infinite-slope transitions dependent on variables other than <code>time</code>. Smooth the transition so that it is more easily integrated through.</p>

Defect	Description
<p>Epetraext uses bad address in parallel, causing <b>Xyce</b> core dump [bug 1072]</p>	<p>If <b>Xyce</b> is run in parallel on a netlist that is so small that all devices are assigned to the same processor, <b>Xyce</b> can core dump when the processor with no work attempts to access invalid memory.</p> <p><i>Workaround:</i> It is best not to try to run <b>Xyce</b> on very small problems in parallel, as this capability is intended for and optimized for very large problems; small problems should be run in serial. If trying to run medium-sized problems in parallel and these core dumps are observed, try running with Zoltan partitioning and singleton removal turned off:</p> <pre>.OPTIONS LINSOL TR_partition=0 + TR_singleton_filter=0</pre>

Table 3: Known Defects and Workarounds.

## Incompatibilities With Other Circuit Simulators

Issue	Comment
AC Analysis not supported	<b>Xyce</b> does not currently support AC analysis.
.OP is not complete	A .OP netlist will run in <b>Xyce</b> , but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In <b>Xyce</b> the BSIM3 level=9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In <b>Xyce</b> the BSIM SOI (v3.2) level=10. Other simulators have different levels for the BSIM SOI.
Node names vs. device names.	Currently, circuit nodes and devices <b>MUST</b> have different names in <b>Xyce</b> . Some simulators can handle a device and a node with the same name, but <b>Xyce</b> cannot.
Interactive mode.	<b>Xyce</b> does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources."	These are not currently supported within <b>Xyce</b> . <i>However...</i> <b>Xyce</b> does support "IC=<value>" statements for capacitors, inductors, and the two BSIM devices which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for .STEP is different.	The manner of specifying a model parameter to be swept is slightly different. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

## Important Changes to **Xyce** Usage Since the Release 5.1.

Table 5 lists some usage changes for **Xyce**.

Issue	Comment
<p>New parameter added to rad-aware models.</p>	<p>In all versions of <b>Xyce</b> prior to Release 5.1.1, the rad-effects models had some terms in the photocurrent that inappropriately depended on the global <code>GMIN</code> setting. For very small devices, these terms were found to dominate the real effects. This dependence has now been replaced with a dependence on a device-specific parameter <code>TFGMIN</code> that defaults to zero. We have found that for most existing large-device examples, this change has negligible effect, while for small devices it eliminates the non-physical <code>GMIN</code>-dependent behavior. Should the user wish to produce results that are exactly compatible with prior releases, simply add a setting of <code>TFGMIN=1e-12</code> to each model card for a rad-aware device. The <code>TFGMIN</code> parameter should be considered deprecated, and may be removed along with the terms dependent on it in a future release.</p>

Table 5: Changes to netlist specification since the last release.

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**Xyce's** expression library is based on that inside Spice 3F5 developed by the EECS Department at the University of California.

The EKV3 MOSFET model was developed by the EKV Team of the Electronics Laboratory-TUC of the Technical University of Crete.

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