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Xyce™ Parallel Electronic Simulator Release Notes

Release 4.1

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Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements
- Any defects fixed since the last release

- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at <http://www.cs.sandia.gov/xyce>.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 4.1.

Supported Platforms (Certified Support)

Xyce 4.1 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 4.1 release.

- Red Hat Enterprise Linux® 4, x86 and x86-64 (serial and parallel)
- Microsoft Windows XP Professional®, x86 (serial)
- Apple® OS X, x86 (serial and parallel)
- NWCC (spirit) (serial and parallel)
- Thunderbird (serial and parallel)
- Xyce directly coupled to the Dakota optimization and uncertainty quantification library for Apple OS X and Linux platforms.

Build Supported Platforms (not Certified)

The platforms listed in this section are “not supported” in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 4.1 release.

- FreeBSD 6.3 on Intel Pentium® architectures (serial and parallel)
- Apple® OS X, PPC (serial and parallel)
- ICC (shasta) (serial and parallel)

Please contact the Xyce development team for platform and configuration availability.

Hardware Requirements

The following are estimated hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*
- 50MB disk space (not including space needed for output files)

Software Requirements

Several libraries are required to run **Xyce** or build **Xyce** from source on a platform. Serial versions of the static **Xyce** binary have no run-time software requirements. However, parallel versions require the following software at run time:

- Open MPI (<http://www.open-mpi.org/>) (version 1.2.5 or higher)
- Intel (<http://www.intel.com/>) MKL (version 10.0) and Compilers (version 10.1)
- NWCC (spirit) and Thunderbird (tbird) users can load the **xyce** module to properly set the environment

Several libraries (all freely available from Sandia National Laboratories or other sites) are always required when building **Xyce** from source. These are:

- Trilinos Solver Library version 8.0 (Sandia, <http://software.sandia.gov/Trilinos>) . This is a suite of libraries including Amesos, AztecOO, Belos, Teuchos, Epetra, EpetraExt, Ifpack, NOX, LOCA.
- SuperLU (libsuperlu.a) (<http://www.nersc.org>)
- UMFPACK version 4.1 and AMD version 1.0 (libumfpack.a, libamd.a) (<http://www.cise.ufl.edu/research/sparse/umfpack/>)
- LAPACK (liblapack.a).
- BLAS (libblas.a).

For parallel builds, the following libraries are additionally required:

- MPI (<http://www.open-mpi.org>) library for message passing (version 1.1 or higher). The version used to build Xyce must be the same that is used for building Trilinos.
- Zoltan version 3.0 (Sandia, <http://www.cs.sandia.gov/Zoltan>) and its associated libraries (libzoltan.a, libzoltanCPP.a, libparmetis.a, libmetis.a)

Xyce Release 4.1 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. Some of this documentation is in “Draft” mode and is incomplete.

- **Xyce** Users’ Guide, Version 4.1
- **Xyce** Reference Guide, Version 4.1
- **Xyce** Release Notes, Version 4.1
- **Xyce** Theory Document
- **Xyce** Test Plan

New Features and Enhancements

Xyce Release 4.1 is the first major release since our Release 4.0.2.

Highlights for this release include:

- Additional SPICE MOSFET levels (levels 2 and 6).
- Addition of a new suite of preprocessing commands which augment netlist files so as to reduce/eliminate common matrix singularities (see “Interface Improvements,” below, for a description).
- Support for simulation of electromechanical and magnetically driven machines with an “accelerated mass device” and time-dependent mutual inductance.
- A $DDX(f(x),x)$ function was added to the expression library, allowing the user to compute the partial derivative of an expression with respect to an independent variable.
- New stand-alone physics-based neutron model.
- Several new photocurrent models, including the level=11, 21, and 23.

For details of each of these new features, see the **Xyce** Users’ Guide, and the **Xyce** Reference Guide.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 4.1.

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements
Resistor (Level 1)	Semiconductor
Resistor (Level 2)	Thermal Resistor
Diode (Level 1)	
Diode (Level 2)	Addition of PSPICE enhancements
Diode (Level 3)	Prompt and delayed photocurrent radiation model
Diode (Level 4)	Generic photocurrent source model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Current Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2)	Prompt photocurrent radiation model
Bipolar Junction Transistor (BJT) (Level 3)	Neutron-effects model
Bipolar Junction Transistor (BJT) (Level 4)	Prompt photocurrent radiation model (same as level 2)
Bipolar Junction Transistor (BJT) (Level 5)	Deveney-Wrobel Neutron model, with photocurrent
Bipolar Junction Transistor (BJT) (Level 6)	Physics-based (QASPR) Neutron model, with photocurrent
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model

Device	Comments
MESFET	
MOSFET (Level 1)	
MOSFET (Level 2)	New! Spice level 2 MOSFET
MOSFET (Level 3)	
MOSFET (Level 6)	New! Spice level 6 MOSFET
MOSFET (Level 9)	BSIM3 model with initial condition support
MOSFET (Level 10)	BSIM SOI model with initial condition support
MOSFET (Level 11)	New! BSIM SOI model with Transient Photocurrent
MOSFET (Level 14)	BSIM4 model
MOSFET (Level 18)	VDMOS general model
MOSFET (Level 19)	VDMOS total dose radiation model
MOSFET (Level 20)	VDMOS photocurrent model
MOSFET (Level 21)	New! Level 1 with photocurrent
MOSFET (Level 23)	New! Level 3 with photocurrent
Transmission Line	Lossless
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled
Generic Switch (SW)	Controlled by an expression
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional
Digital (Level 1)	Behavioral Digital
EXT (Level 1)	External device, used for code coupling and power-node parasitics simulations
OP AMP (Level 1)	Ideal operational amplifier
ACC	Accelerated mass device, used for simulation of electromechanical and magnetically-driven machines
NEUTRON (Level 1)	New! Stand-alone neutron device model

Table 1: Devices Supported by Xyce

New Devices

- Additional SPICE MOSFET levels (level=2 and level=6).
- Level=11 MOSFET (BSIM SOI plus photocurrent)
- Level=21 MOSFET (SPICE level=1 MOSFET plus photocurrent)
- Level=23 MOSFET (SPICE level=3 MOSFET plus photocurrent)

- Stand-alone physics-based neutron model. (same physics as the level=6 BJT)

Enhanced Solver Stability and Features

- Enhanced non-LTE based step-size selection strategy. The Non LTE strategy used in Xyce is based on success of the nonlinear solve. This strategy is enabled by setting ERROPTION=1. The behavior of erroption=1 is slightly different for the BDF15 integrator and the Trapezoid integrator.
 - For the BDF15 integrator, if the nonlinear solver converges then the step-size is doubled. On the other hand, if the nonlinear solver fails to converge, then the step-size is cut by one eighth.
 - For the Trapezoid integrator, the options are slightly more refined. If the number of nonlinear iterations is below NLMIN, then the step-size is doubled. If the number of nonlinear iterations is below NLMAX then the step-size is cut by one eighth. In between, the step-size is left alone.

See the Xyce User's Guide for a complete description.

- Trapezoidal method is now supported. By default, Local truncation error control is used and normally works fine. One feature of the Trapezoid integrator is that strong ringing will occur when discontinuities are introduced by sources or models. This ringing is entirely artificially introduced by the numerical algorithm. In this case, using a Non LTE strategy may help.

Please refer to Users Guide Chapter 7.2 Section "Transient Time Step Selection Advice" for detailed instruction on how to use Trapezoidal method, especially with non LTE time step control strategy.

Interface Improvements

- Introduction of a new set of .PREPROCESS commands to add the following features:
 - **Ground synonym replacement.** Xyce can now treat the keywords GND, GND!, GROUND, or any lowercase/capital variation thereof as synonyms for node 0.
 - **Removal of Unused Components.** Xyce can now automatically remove devices from a netlist for which all device terminals are connected to the same node (e.g., a resistor whose terminals are both connected to node 1).
 - **Automatic addition of resistors to dangling nodes.** Xyce can now automatically produce a new netlist file which contains a set of resistors (whose value is specified by the user) which connect to ground all nodes which are connected to only one device terminal and/or all nodes which have no DC path to ground

See the Xyce User's Guide for a complete description.

Defects of Release 4.0.2 Fixed in this Release

Defect	Description
[Bug 1367] Make .OPTIONS TIMEINT ERROPTION work for new-DAE	ERROPTION=1 is a time stepping option that forces the time integrator to ignore local truncation error, both for determining step success/failure, and also changing the stepsize. If enabled, it only considers success and/or failure of the nonlinear solver, and other constraints such as the maximum time step when determining the stepsize. Prior to this release, this option only worked for the old time integrator. It now works for both the new (newdae=1) and old (newdae=0) time integrators
[Bug 22 SON] Mutual Inductor Problems with netlists lacking .END statement	It was discovered that mutual inductors were not properly being instantiated in circuit netlists lacking a .END statement. This has now been fixed so that mutual inductors are instantiated whether or not a .END statement is present in the netlist file.
[Bug 24 SON] BSIM4 rbodymod errors	Versions of Xyce prior to this release had a bug in the handling of the substrate resistance network when the parameter RBODYMOD was set to a non-zero value. This bug has been fixed in Release 4.1.
[Bug 1471] Temperature interpolation broken for level 1 and 3 MOSFET	In previous releases of Xyce , the quadratic temperature interpolation feature was not working in the levels 1 and 3 MOSFET. In this release, temperature interpolation is correctly implemented for levels 1, 2, 3, 6, 10, and 18. It remains unimplemented for the level 9 (BSIM3) and 14 (BSIM4).
[Bug 1376] Case sensitivity of ON and OFF parameters	In previous releases of Xyce , the ON and OFF parameters of the BJT and Switch devices worked as specified in the Reference Guide only if the parameter was given in all upper-case letters, and would generate an error message if given in lower case. As of this release, the parameter is case-insensitive and may be given in any combination of upper- and lower-case.
[Bug 1576] Level 23 MOSFET numerical errors	A bug in the handling of the level 23 and level 21 MOSFETS when FUNCTIONTYPE was set to zero led to severe convergence problems. These have been fixed.
[Bug 1461] MOSFET devices do not support OFF parameter	Until this release of Xyce , the OFF parameter for MOSFETS was unsupported. Support for this parameter, compatible with SPICE3F5, is included in this release of Xyce for the MOSFET levels 1, 2, 3, 6, 9, 10, 14, 21, and 23.

Defect	Description
[Bug 1578] Invalid first character of a line led to unhelpful error message	Until this release of Xyce , a netlist error in which the first character of a line did not correspond to a valid device type would lead to an error message that did not help the user locate the netlisting error. This type of problem was typically seen when the asterisk (*) was omitted before a comment line, or the leading "." was accidentally deleted from a .PRINT line. Xyce now prints a helpful message that includes the line on which the error was found.

Table 2: Fixed Defects.

Known Defects and Workarounds

Defect	Description
<p>Connectivity checking is broken for devices with more than 10 leads [SON Bug 37]</p>	<p>Late in the release process for Xyce Release 4.1 it was discovered that the code that checks circuit topology for basic errors such as a node having no DC path to ground or a node being connected to only one device has a bug in it that causes the code to emit a cryptic error message, “Internal: lead index not found” after which the code will exit. This error has so far only been seen when a user has attempted to connect a large number of inductors together using multiple mutual inductor lines. The maximum number of non-ground leads that can be used without confusing this piece of code is 10. If you see the error message “Internal: lead index not found.” and you have such a large mutual inductor, this bug is the source of the problem. <i>Workaround:</i> Disable connectivity checking by adding the line</p> <pre data-bbox="716 957 1240 982">.OPTIONS TOPOLOGY CHECK_CONNECTIVITY=0</pre> <p>to your netlist. This will disable the check for the basic errors such as floating nodes and improperly connected devices, but will allow the netlist to run with a highly-connected mutual inductor.</p>
<p>AC parameter on voltage sources broken [bug 1302]</p>	<p>Xyce does not support AC analysis, but its parser does recognize and attempt to process the AC keyword and its parameter that other simulators support on voltage source lines. Instead of emitting a helpful error message, Xyce will report an invalid parameter ACMAG with no guidance to point the user to the line of the netlist with the problem. <i>Workaround:</i> Do not use the AC keyword and its magnitude parameter (the number immediately following the keyword) on a voltage source line.</p>
<p>.DC sweep output.</p>	<p>.DC sweep calculation does not automatically output sweep results. <i>Workaround:</i> Use .PRINT statement to output sweep variable results.</p>
<p>BJT Current Crowding</p>	<p>“Timestep too small” failures can result when IRB nonzero with level 2 and level 4 BJT <i>Workaround:</i> If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the Xyce development team so that this bug can be characterized and eliminated.</p>

Defect	Description
<p>Microsoft Windows installation restrictions</p>	<p>Users with insufficient privileges (i.e. Limited Account) are not permitted to install Xyce into folders on the System Drive (usually C:). <i>Workaround:</i> First, manually create the desired folder on the System Drive. It is then possible to install Xyce into this folder by following the standard Setup procedure.</p>
<p>Incompatible proprietary file formats.</p>	<p>Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in Xyce. Xyce does not recognize proprietary file formats. <i>Workaround:</i> It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.</p>
<p>One known instance of restart results not matching original run results.</p>	<p>There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range. <i>Workaround:</i> The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.</p>
<p>Lead currents in B/E/F/G/H source and switch expressions [bug 801]</p>	<p>Use of lead currents in B/E/F/G/H source and switch expressions will lead to incorrect results. A fatal diagnostic should be generated for such usage, but is not. The only supported use of lead currents is on .PRINT lines in Xyce 3.1.</p>

Defect	Description
<p>Infinite-slope transitions in B-sources causes "time step too small" errors [bug 772]</p>	<p>The nonlinear dependent source ("B-source") allows the user to specify expressions that could have infinite-slope transitions, such as</p> <pre>Bcrt1 OUTA 0 V={ IF((V(IN) > 3.5), 5, 0) }</pre> <p>This can lead to "timestep too small" errors when Xyce reaches the transition point. Infinite-slope transitions in expressions dependent only on the <code>time</code> variable are a special case, because Xyce can detect that they are going to happen in the future and set a "breakpoint" to capture them. Infinite-slope transitions depending on other solution variables cannot be predicted in advance, and cause the time integrator to scale back the timestep repeatedly in an attempt to capture the feature until the timestep is too small to continue.</p> <p><i>Workaround:</i> Do not use step-function or other infinite-slope transitions dependent on variables other than <code>time</code>. Smooth the transition so that it is more easily integrated through.</p>
<p>Epetraext uses bad address in parallel, causing Xyce core dump [bug 1072]</p>	<p>If Xyce is run in parallel on a netlist that is so small that all devices are assigned to the same processor, Xyce can core dump when the processor with no work attempts to access invalid memory.</p> <p><i>Workaround:</i> It is best not to try to run Xyce on very small problems in parallel, as this capability is intended for and optimized for very large problems; small problems should be run in serial. If trying to run medium-sized problems in parallel and these core dumps are observed, try running with Zoltan partitioning and singleton removal turned off:</p> <pre>.OPTIONS LINSOL TR_partition=0 + TR_singleton_filter=0</pre>

Defect	Description
<p>On some circuits the new time integrator gets time-step-too-small failures.</p>	<p><i>Workaround:</i> This is not really a “defect” in that this can happen with any time integrator. However, as the new time integrator is a new capability, it has had less time to mature than the old time integrator (which was the default in Xyce for 6 years). If you have a circuit that ran fine in a previous version of Xyce, but is getting a time-step-too-small failure in Xyce 4.1, the new time integrator might be the culprit. If you set the following option:</p> <pre>.OPTIONS TIMEINT maxord=1</pre> <p>This will force the new time integrator to function similarly to the old one by using only a fixed first-order integration method instead of its variable-order (first-through fifth-order) method. If this doesn't work, try this:</p> <pre>.OPTIONS TIMEINT newdae=0</pre> <p>Setting this option will force Xyce 4.1 to use to old time integrator. Please note that the old time integrator will be removed from Xyce in a future release, and therefore it is important that the development team be made aware of bugs that require users to fall back on the old time integrator so that we can address the problem before removing the old integrator. If you are forced to use “newdae=0” to get your circuit to work, please file a bug report on the project's issue tracker, “bugzilla.”</p>

Table 3: Known Defects and Workarounds.

Incompatibilities With Other Circuit Simulators

Issue	Comment
AC Analysis not supported	Xyce does not currently support AC analysis. The current version does, however, have a bug in the voltage source that causes a fairly unhelpful error message to be emitted if the user specifies an AC magnitude on the voltage source line, such as AC 0. The error message will mention an invalid parameter ACMAG. If you see this message, remove all references to the AC magnitude on any voltage sources in your netlist.
.OP is not complete	A .OP netlist will run in Xyce , but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In Xyce the BSIM3 level=9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In Xyce the BSIM SOI (v3.2) level=10. Other simulators have different levels for the BSIM SOI.
BSIM4 level.	In Xyce the BSIM4 level=14. Other simulators have different levels for the BSIM4 (in Hspice, level =54).
Node names vs. device names.	Currently, circuit nodes and devices MUST have different names in Xyce . Some simulators can handle a device and a node with the same name, but Xyce cannot.
Interactive mode.	Xyce does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources."	These are not currently supported within Xyce . <i>However...</i> Xyce does support "IC=<value>" statements for capacitors, inductors, and the two BSIM devices which will automatically set these voltage drops at the beginning of a transient simulation.

Issue	Comment
Syntax for .STEP is different.	The manner of specifying a model parameter to be swept is slightly different. Also, it is not possible to do a .STEP sweep over a global parameter. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

Important Changes to Xyce Usage Since the Last Release.

Table 5 lists some usage changes for Xyce.

Issue	Comment
Variable Mutual inductance coupling	As of Release 4.1 of Xyce, the coupling parameter for the linear mutual inductor may be an expression (enclosed in curly braces) that may depend explicitly on time or on other solution variables. Prior to this release, it was required to be a constant.

Table 5: Changes to netlist specification since the last release.

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