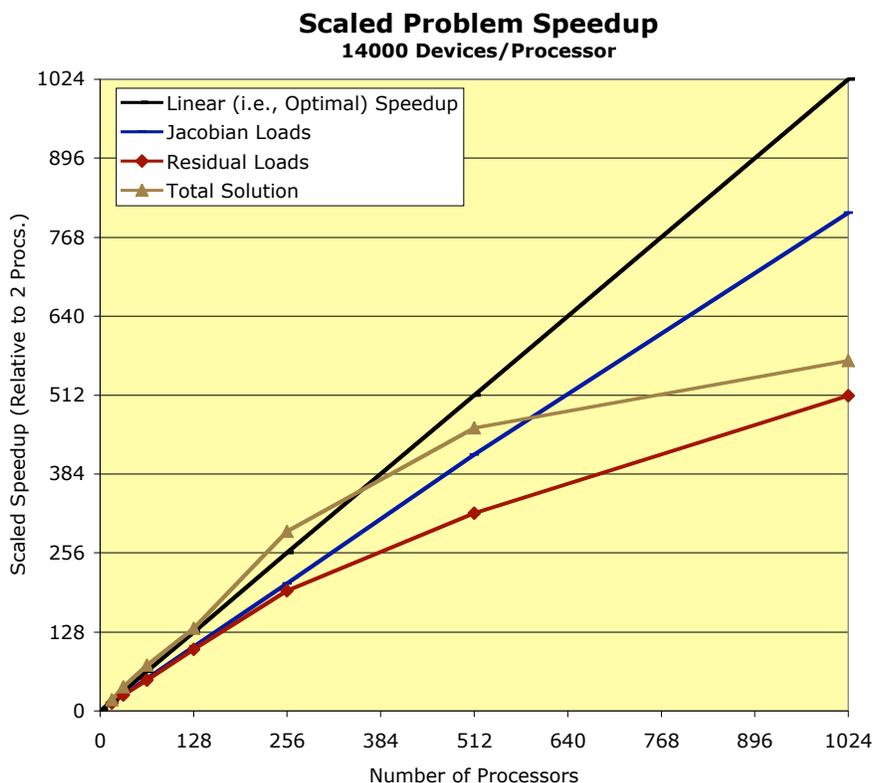


# Xyce™ Parallel Electronic Simulator

## News Note

### Largest Full, Analog Circuit Ever Run<sup>□</sup>



**Figure 1.** Scaled speedup for nonlinear transmission line problem. NOTE: the scaled-speedup numbers are with respect to two-processors, the smallest number used for the study. Also, the “Total Solution” scaling includes the effects of problem-dependent algorithmic scaling.

On May 25<sup>th</sup>, 2003, the Xyce<sup>□</sup> team at Sandia National Laboratories ran a 14,336,000 device circuit problem using 1024 processors of Lawrence Livermore’s ASCI White IBM computer. To the best of the team’s ability to determine, this is the largest full, analog circuit simulation ever run *and* it was run on the largest number of concurrent processors ever used for circuit simulation. This simulation resulted in a linear system of approximately 6,000,000 unknowns that were solved using Sandia’s Trilinos solver toolkit (the AztecOO Krylov

<sup>□</sup> To the best of the team’s knowledge of the available literature.

solver, specifically).

The circuit was comprised of repeated blocks of a nonlinear transmission line problem, replicated and coupled to provide each processor with 14,000 devices for each calculation. The transient calculation computed the voltage and current behavior of the circuit for a specified length of simulation time.

## About Xyce<sup>□</sup>

**Xyce** is a new circuit simulation code designed from the ground-up as a parallel tool in the most general sense, that is, a message passing parallel implementation, which allows it to run efficiently on the widest possible number of computing platforms. These include serial, shared-memory and distributed-memory parallel as well as heterogeneous platforms.

An ASCI funded project, the **Xyce** Parallel Electronic Simulator development has focused on improving the capability over the current state-of-the-art in the following areas:

- Capability to solve extremely large circuit problems by supporting large-scale parallel computing platforms (up to thousands of processors). Note that this includes support for most popular parallel and serial computers.
- Improved performance for all numerical kernels (e.g., time integrator, nonlinear and linear solvers) through state-of-the-art algorithms and novel techniques.
- Support for modeling circuit phenomena at a variety of abstraction levels (device, analog, digital and mixed-signal) in a rigorous and tightly coupled manner, allowing for timely, full-system solutions.
- Object-oriented code design and implementation using modern coding-practices that ensure that the **Xyce** Parallel Electronic Simulator will be maintainable and extensible far into the future.
- Improved “useability” through improved analysis control (e.g., variable solution checkpoint/restart capability) that improves the design workflow.

For more information on **Xyce**, please visit its external web site at

<http://www.cs.sandia.gov/Xyce>

## About Trilinos

The Trilinos Project is an effort to develop and implement robust parallel algorithms using modern object-oriented software design, while still leveraging the value of established numerical libraries such as PETSc, Aztec, the BLAS and LAPACK. It emphasizes abstract interfaces for maximum flexibility of component interchanging, and provides a full-featured set of concrete classes that implement all abstract interfaces.

For more information on Trilinos, please see <http://software.sandia.gov/trilinos>

About ASCI White (from <http://www.llnl.gov/asci/platforms/white/>)

ASCI White is the third step in the DOE's five stage Accelerated Strategic Computing Initiative (ASCI) plan to achieve a 100 TeraOP/s supercomputer system by 2004. It is part of the DOE's science-based Stockpile Stewardship Program to maintain the safety and reliability of the US nuclear stockpile without underground testing.

ASCI White is actually comprised of three separate systems based upon IBM's POWER3 SP technology. The largest system is a 512 node SMP (16 CPUs/node) system that is currently ranked as the world's fastest computer, with a peak speed slightly greater than 12 TeraOP/s.

For more information on ASCI White, please see <http://www.llnl.gov/asci/platforms/white/>

## Trademark Information

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## Contacts

Email <mailto:xyce-support@sandia.gov>

World Wide Web <http://www.cs.sandia.gov/Xyce>

